XILINX

IMPORTANT NOTICE
All new designs should use XC3000A or XC3100A. Information on XC3000 and XC3100 is presented here as reference for existing designs.

XC3000, XC3000A, XC3000L, XC3100, XC3100A Logic Cell Array Families

Product Description

Features

- Complete line of five related Field Programmable Gate Array product families
  - XC3000, XC3000A, XC3000L, XC3100, XC3100A
- Ideal for a wide range of custom VLSI design tasks
  - Replaces TTL, MSI, and other PLD logic
  - Integrates complete sub-systems into a single package
  - Avoids the NRE, time delay, and risk of conventional masked gate arrays
- High-performance CMOS static memory technology
  - Guaranteed toggle rates of 70 to 325 MHz, logic delays from 9 to 2.2 ns
  - System clock speeds over 80 MHz
  - Low quiescent and active power consumption
- Flexible FPGA architecture
  - Compatible arrays ranging from 1,000 to 7,500 gate complexity
  - Extensive register, combinatorial, and I/O capabilities
  - High fan-out signal distribution, low-skew clock nets
  - Internal 3-state bus capabilities
  - TTL or CMOS input thresholds
  - On-chip crystal oscillator amplifier
- Unlimited reprogrammability
  - Easy design iteration
  - In-system logic changes
- Extensive Packaging Options
  - Over 20 different packages
  - Plastic and ceramic surface-mount and pin-grid-array packages
  - Thin and Very Thin Quad Flat Pack (TQFP and VQFP) options
- Ready for volume production
  - Standard, off-the-shelf product availability
  - 100% factory pre-tested devices
  - Excellent reliability record
- Complete XACT Development System
  - Schematic capture, automatic place and route
  - Logic and timing simulation
  - Interactive design editor for design optimization
  - Timing calculator
  - Interfaces to popular design environments like Viewlogic, Cadence, Mentor Graphics, and others

Description

The CMOS XC3000 Class of Logic Cell Array (LCA) families provide a group of high-performance, high-density, digital integrated circuits. Their regular, extendable, flexible, user-programmable array architecture is composed of a configuration program store plus three types of configurable elements: a perimeter of I/O Blocks (IOBs), a core array of Configurable Logic Bocks (CLBs) and resources for interconnection. The general structure of an LCA device is shown in Figure 1 on the next page. The XACT development system provides schematic capture and auto place-and-route for design entry. Logic and timing simulation, and in-circuit emulation are available as design verification alternatives. The design editor is used for interactive design optimization, and to compile the data pattern that represents the configuration program.

The LCA user logic functions and interconnections are determined by the configuration program data stored in internal static memory cells. The program can be loaded in any of several modes to accommodate various system requirements. The program data resides externally in an EEPROM, EPROM or ROM on the application circuit board, or on a floppy disk or hard disk. On-chip initialization logic provides for optional automatic loading of program data at power-up. The companion XC17XX Serial Configuration PROMs provide a very simple serial configuration program storage in a one-time programmable package.

Device	CLBs	Array	User I/Os Max	Flip-Flops	Horizontal Longlines	Configuration Data Bits
XC3020, 3020A, 3020L, 3120, 3120A	64	8 x 8	64	256	16	14,779
XC3030, 3030A, 3030L, 3130, 3130A	100	10 x 10	80	360	20	22,176
XC3042, 3042A, 3042L, 3142, 3142A	144	12 x 12	96	480	24	30,784
XC3064, 3064A, 3064L, 3164, 3164A	224	16 x 14	120	688	32	46,064
XC3090, 3090A, 3090L, 3190, 3190A	320	16 x 20	144	928	40	64,160
XC3195, 3195A	484	22 x 22	176	1,320	44	94,984

The XC3000 Logic Cell Array families provide a variety of logic capacities, package styles, temperature ranges and speed grades.

Architecture

The perimeter of configurable IOBs provides a programmable interface between the internal logic array and the device package pins. The array of CLBs performs user-specified logic functions. The interconnect resources are programmed to form networks, carrying logic signals among blocks, analogous to printed circuit board traces connecting MSI/SSI packages.

The block logic functions are implemented by programmed look-up tables. Functional options are implemented by program-controlled multiplexers. Interconnecting networks between blocks are implemented with metal segments joined by program-controlled pass transistors.

These LCA functions are established by a configuration program which is loaded into an internal, distributed array of configuration memory cells. The configuration program is loaded into the LCA device at power-up and may be reloaded on command. The Logic Cell Array includes logic and control signals to implement automatic or passive configuration. Program data may be either bit serial or byte parallel. The XACT development system generates the configuration program bitstream used to configure the LCA device. The memory loading process is independent of the user logic functions.

Configuration Memory

The static memory cell used for the configuration memory in the Logic Cell Array has been designed specifically for high reliability and noise immunity. Integrity of the LCA device configuration memory based on this design is assured even under adverse conditions. Compared with other programming alternatives, static memory provides the best combination of high density, high performance, high reliability and comprehensive testability. As shown in Figure 2, the basic memory cell consists of two CMOS inverters plus a pass transistor used for writing and reading cell data. The cell is only written during configuration and only read during readback. During normal operation, the cell provides continuous control and the pass transistor is off and does not affect cell stability. This is quite different from the operation of conventional memory devices, in which the cells are frequently read and rewritten.

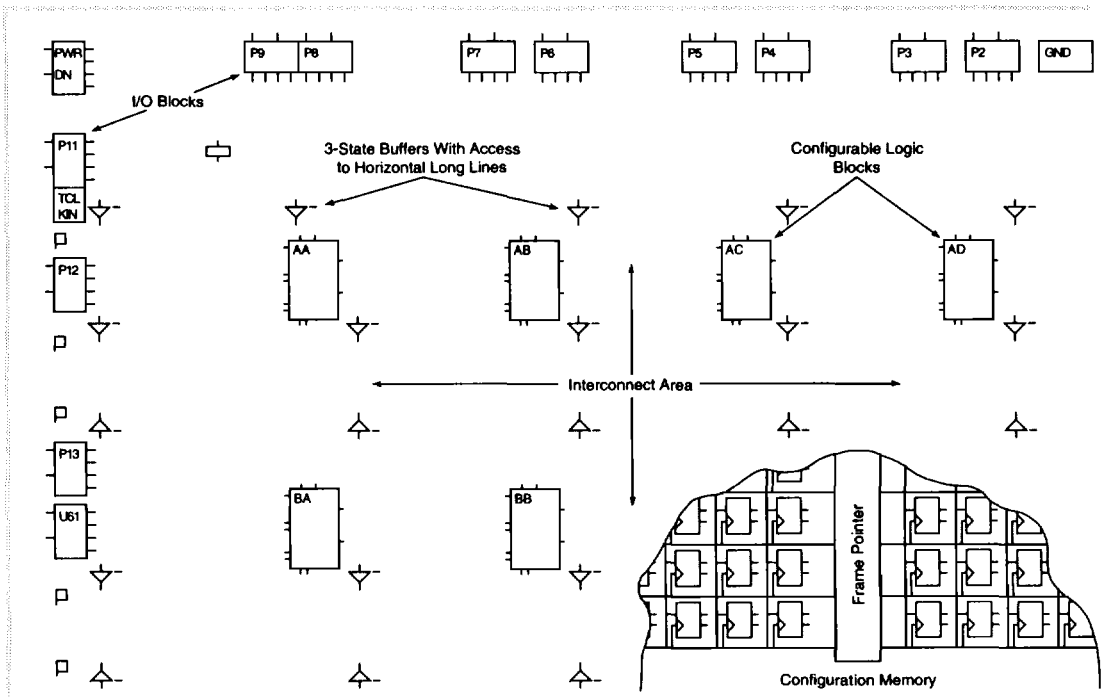


Figure 1. Logic Cell Array Structure.

It consists of a perimeter of programmable I/O blocks, a core of configurable logic blocks and their interconnect resources. These are all controlled by the distributed array of configuration program memory cells.

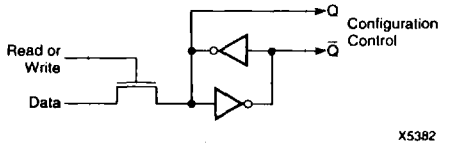


Figure 2. Static Configuration Memory Cell.
It is loaded with one bit of configuration program and controls one program selection in the Logic Cell Array.

The memory cell outputs Q and $\overline{Q}$ use ground and V_{CC} levels and provide continuous, direct control. The additional capacitive load together with the absence of address decoding and sense amplifiers provide high stability to the cell. Due to the structure of the configuration memory cells, they are not affected by extreme power-supply excursions or very high levels of alpha particle radiation. In reliability testing, no soft errors have been observed even in the presence of very high doses of alpha radiation.

The method of loading the configuration data is selectable. Two methods use serial data, while three use byte-wide data. The internal configuration logic utilizes framing information, embedded in the program data by the XACT development system, to direct memory-cell loading. The serial-data framing and length-count preamble provide programming compatibility for mixes of various LCA device devices in a synchronous, serial, daisy-chain fashion.

I/O Block

Each user-configurable IOB shown in Figure 3, provides an interface between the external package pin of the device and the internal user logic. Each IOB includes both registered and direct input paths. Each IOB provides a programmable 3-state output buffer, which may be driven by a registered or direct output signal. Configuration options allow each IOB an inversion, a controlled slew rate and a high impedance pull-up. Each input circuit also provides input clamping diodes to provide electrostatic protection, and circuits to inhibit latch-up produced by input currents.

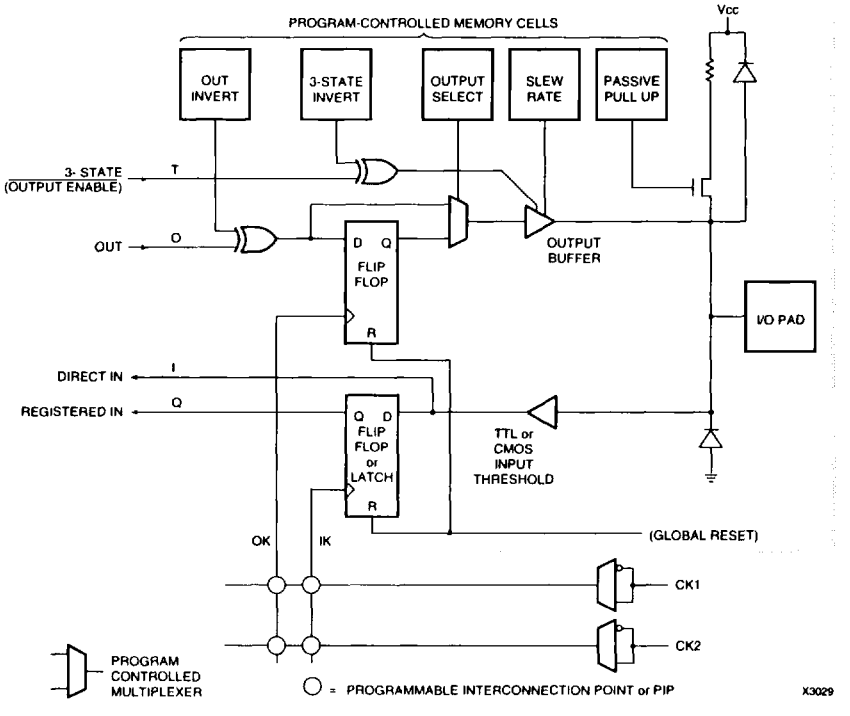


Figure 3. Input/Output Block.
Each IOB includes input and output storage elements and I/O options selected by configuration memory cells. A choice of two clocks is available on each die edge. The polarity of each clock line (not each flip-flop or latch) is programmable. A clock line that triggers the flip-flop on the rising edge is an active Low Latch Enable (Latch transparent) signal and vice versa. Passive pull-up can only be enabled on inputs, not on outputs. All user inputs are programmed for TTL or CMOS thresholds.

The input-buffer portion of each IOB provides threshold detection to translate external signals applied to the package pin to internal logic levels. The global input-buffer threshold of the IOBs can be programmed to be compatible with either TTL or CMOS levels. The buffered input signal drives the data input of a storage element, which may be configured as either a flip-flop or a latch. The clocking polarity (rising/falling edge-triggered flip-flop, High/Low transparent latch) is programmable for each of the two clock lines on each of the four die edges. Note that a clock line driving a *rising* edge-triggered flip-flop makes any latch driven by the same line on the same edge *Low*-level transparent and vice versa (*falling* edge, *High* transparent). All Xilinx primitives in the supported schematic-entry packages, however, are positive edge-triggered flip-flops or High transparent latches. When one clock line must drive flip-flops as well as latches, it is necessary to compensate for the difference in clocking polarities with an additional inverter either in the flip-flop clock input or the latch-enable input. I/O storage elements are reset during configuration or by the active-Low chip $\overline{\text{RESET}}$ input. Both direct input (from IOB pin I) and registered input (from IOB pin Q) signals are available for interconnect.

For reliable operation, inputs should have transition times of less than 100 ns and should not be left floating. Floating CMOS input-pin circuits might be at threshold and produce oscillations. This can produce additional power dissipation and system noise. A typical hysteresis of about 300 mV reduces sensitivity to input noise. Each user IOB includes a programmable high-impedance pull-up resistor, which may be selected by the program to provide a constant High for otherwise undriven package pins. Although the Logic Cell Array provides circuitry to provide input protection for electrostatic discharge, normal CMOS handling precautions should be observed.

Flip-flop loop delays for the IOB and logic-block flip-flops are about 3 ns. This short delay provides good performance under asynchronous clock and data conditions. Short loop delays minimize the probability of a metastable condition that can result from assertion of the clock during data transitions. Because of the short-loop-delay characteristic in the Logic Cell Array, the IOB flip-flops can be used to synchronize external signals applied to the device. Once synchronized in the IOB, the signals can be used internally without further consideration of their clock relative timing, except as it applies to the internal logic and routing-path delays.

IOB output buffers provide CMOS-compatible 4-mA source-or-sink drive for high fan-out CMOS or TTL-compatible signal levels (8 mA in the XC3100 family). The network driving IOB pin O becomes the registered or direct data source for the output buffer. The 3-state control signal (IOB) pin FT can control output activity. An open-drain output may be obtained by using the same signal for driving the output and 3-state signal nets so that the buffer output is enabled only for a Low.

Configuration program bits for each IOB control features such as optional output register, logic signal inversion, and 3-state and slew-rate control of the output.

The program-controlled memory cells of Figure 3 control the following options.

- Logic **inversion of the output** is controlled by one configuration program bit per IOB.

- Logic **3-state control** of each IOB output buffer is determined by the states of configuration program bits which turn the buffer on, or off, or select the output buffer 3-state control interconnection (IOB pin T). When this IOB output control signal is High, a logic one, the buffer is **disabled** and the package pin is high impedance. When this IOB output control signal is Low, a logic zero, the buffer is **enabled** and the package pin is active. Inversion of the buffer 3-state control-logic sense (output enable) is controlled by an additional configuration program bit.

- **Direct or registered output** is selectable for each IOB. The register uses a positive-edge, clocked flip-flop. The clock source may be supplied (IOB pin OK) by either of two metal lines available along each die edge. Each of these lines is driven by an invertible buffer.

- Increased **output transition speed** can be selected to improve critical timing. Slower transitions reduce capacitive-load peak currents of non-critical outputs and minimize system noise.

- An internal high-impedance **pull-up resistor** (active by default) prevents unconnected inputs from floating.

Summary of I/O Options

- Inputs
  - Direct
  - Flip-flop/latch
  - CMOS/TTL threshold (chip inputs)
  - Pull-up resistor/open circuit
- Outputs
  - Direct/registered
  - Inverted/not
  - 3-state/on/off
  - Full speed/slew limited
  - 3-state/output enable (inverse)

Configurable Logic Block

The array of CLBs provides the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix within the perimeter of IOBs. The XC3020 has 64 such blocks arranged in 8 rows and 8 columns. The XACT development system is used to compile the configuration data which is to be loaded into the internal configuration memory to define the operation and interconnection of each block. User definition of CLBs and their interconnecting networks may be done by automatic translation from a schematic-capture logic diagram or optionally by installing library or user macros.

Each CLB has a combinatorial logic section, two flip-flops, and an internal control section. See Figure 4. There are: five logic inputs (A, B, C, D and E); a common clock input (K); an asynchronous direct RESET input (RD); and an enable clock (EC). All may be driven from the interconnect resources adjacent to the blocks. Each CLB also has two outputs (X and Y) which may drive interconnect networks.

Data input for either flip-flop within a CLB is supplied from the function F or G outputs of the combinatorial logic, or the block input, DI. Both flip-flops in each CLB share the

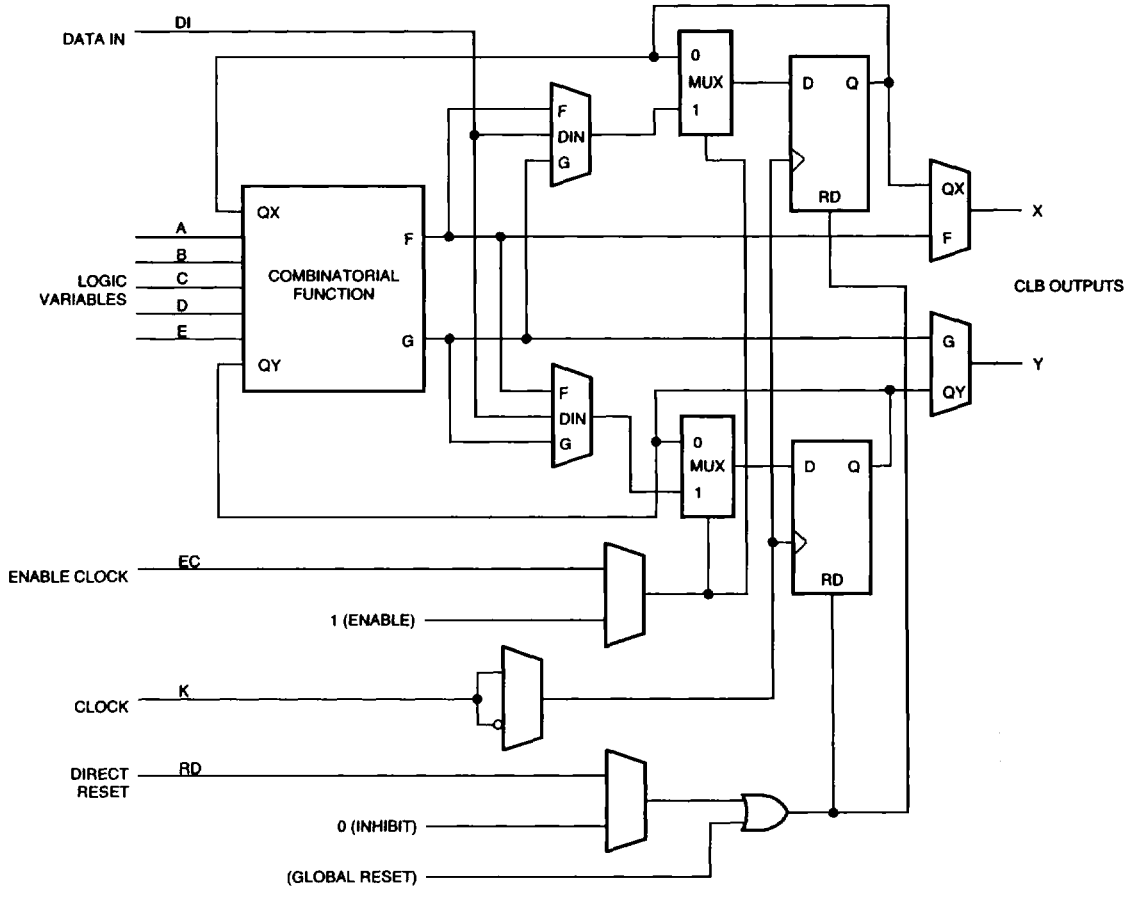


Figure 4. Configurable Logic Block. Each CLB includes a combinatorial logic section, two flip-flops and a program memory controlled multiplexer selection of function. It has.
- five logic variable inputs A, B, C, D, and E
- a direct data in DI
- an enable clock EC
- a clock (invertible) K
- an asynchronous direct RESET RD
- two outputs X and Y

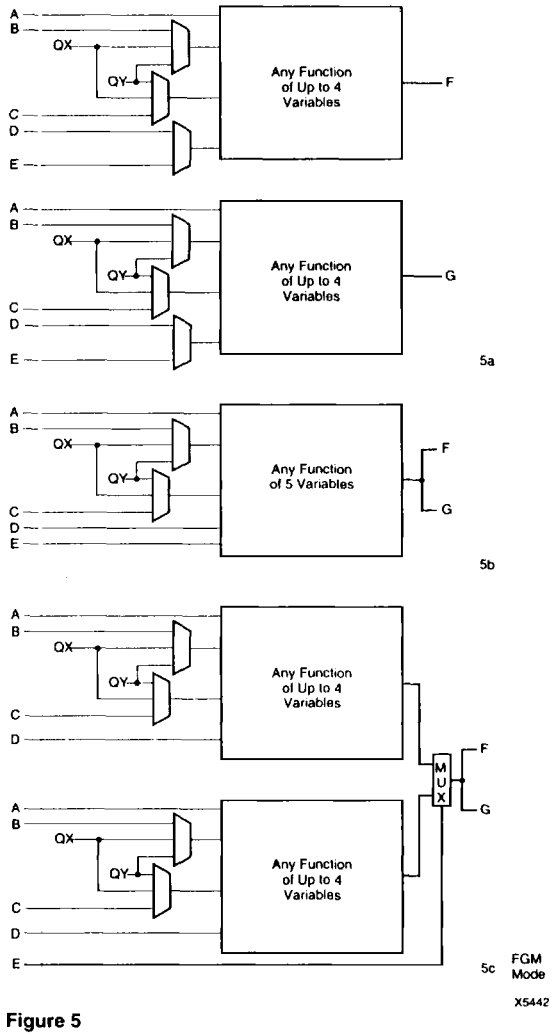


Figure 5

5a. Combinatorial Logic Option FG generates two functions of four variables each. One variable, A, must be common to both functions. The second and third variable can be any choice of of B, C, QX and QY The fourth variable can be any choice of D or E.

5b. Combinatorial Logic Option F generates any function of five variables: A, D, E and and two choices out of B, C, QX, QY.

5c. Combinatorial Logic Option FGM allows variable E to select between two functions of four variables: Both have common inputs A and D and any choice out of B, C, QX and QY for the remaining two variables. Option 3 can then implement some functions of six or seven variables.

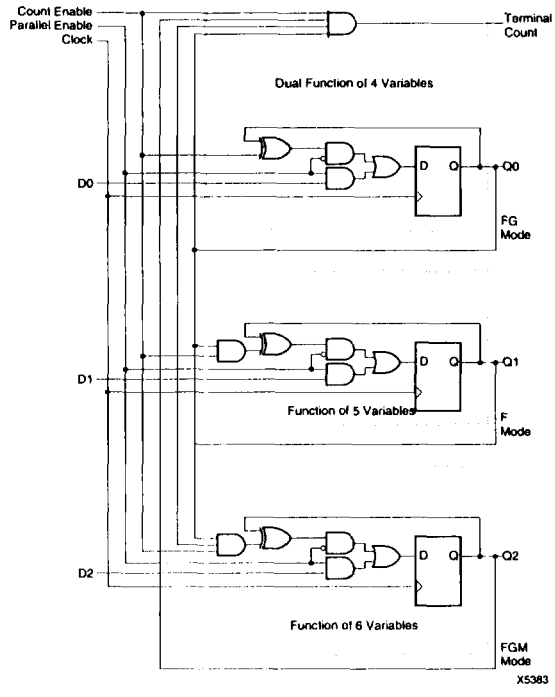


Figure 6. C8BCP Macro.

The C8BCP macro (modulo-8 binary counter with parallel enable and clock enable) uses one combinatorial logic block of each option.

asynchronous RD which, when enabled and High, is dominant over clocked inputs. All flip-flops are reset by the active-Low chip input, $\overline{\text{RESET}}$, or during the configuration process. The flip-flops share the enable clock (EC) which, when Low, recirculates the flip-flops' present states and inhibits response to the data-in or combinatorial function inputs on a CLB. The user may enable these control inputs and select their sources. The user may also select the clock net input (K), as well as its active sense within each CLB. This programmable inversion eliminates the need to route both phases of a clock signal throughout the device. Flexible routing allows use of common or individual CLB clocking.

The combinatorial-logic portion of the CLB uses a 32 by 1 look-up table to implement Boolean functions. Variables selected from the five logic inputs and two internal block flip-flops are used as table address inputs. The combinatorial propagation delay through the network is independent of the logic function generated and is spike free for single input variable changes. This technique can generate two independent logic functions of up to four variables each as shown in Figure 5a, or a single function of five variables as shown in Figure 5b, or some functions of seven variables as shown in Figure 5c. Figure 6 shows a modulo-8 binary counter with parallel enable. It uses one CLB of each type. The partial functions of six or seven variables are implemented using the input variable (E) to dynamically select between two functions of four different variables. For the two functions of four variables each, the independent results (F and G) may be used as data inputs to either flip-flop or either logic block output. For the single function of five variables and merged functions of six or seven variables, the F and G outputs are identical. Symmetry of the F and G functions and the flip-flops allows the interchange of CLB outputs to optimize routing efficiencies of the networks interconnecting the CLBs and IOBs.

Programmable Interconnect

Programmable-interconnection resources in the Logic Cell Array provide routing paths to connect inputs and outputs of the IOBs and CLBs into logic networks. Interconnections between blocks are composed of a two-layer grid of metal segments. Specially designed pass transistors, each controlled by a configuration bit, form programmable interconnect points (PIPs) and switching matrices used to implement the necessary connections between selected metal segments and block pins. Figure 7 is an example of a routed net. The XACT development system provides automatic routing of these interconnections. Interactive routing (Editnet) is also available for design optimization. The inputs of the CLBs or IOBs are multiplexers which can be programmed to select an input network from the adjacent interconnect segments. ***Since the switch connections to block inputs are unidirectional, as are block outputs, they are usable only for block input connection and not for routing.*** Figure 8 illustrates routing access to logic block input variables, control inputs and block outputs. Three types of metal resources are provided to accommodate various network interconnect requirements.

- General Purpose Interconnect
- Direct Connection
- Longlines (multiplexed busses and wide AND gates)

General Purpose Interconnect

General purpose interconnect, as shown in Figure 9, consists of a grid of five horizontal and five vertical metal segments located between the rows and columns of logic and IOBs. Each segment is the height or width of a logic block. Switching matrices join the ends of these segments and allow programmed interconnections between the metal grid segments of adjoining rows and columns. The switches of an unprogrammed device are all non-conducting. The connections through the switch matrix may be established by the automatic routing or by using Editnet to select the desired pairs of matrix pins to be connected or disconnected. The legitimate switching matrix combinations for each pin are indicated in Figure 10 and may be highlighted by the use of the Show-Matrix command in the XACT system.

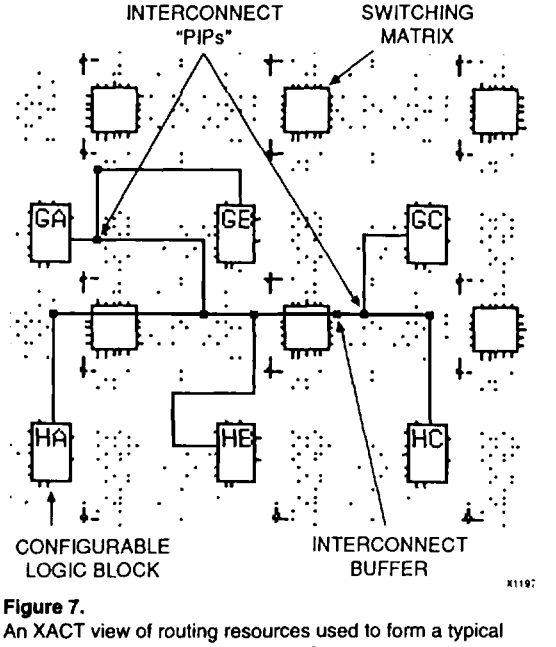


Figure 7.
An XACT view of routing resources used to form a typical interconnection network from CLB GA.

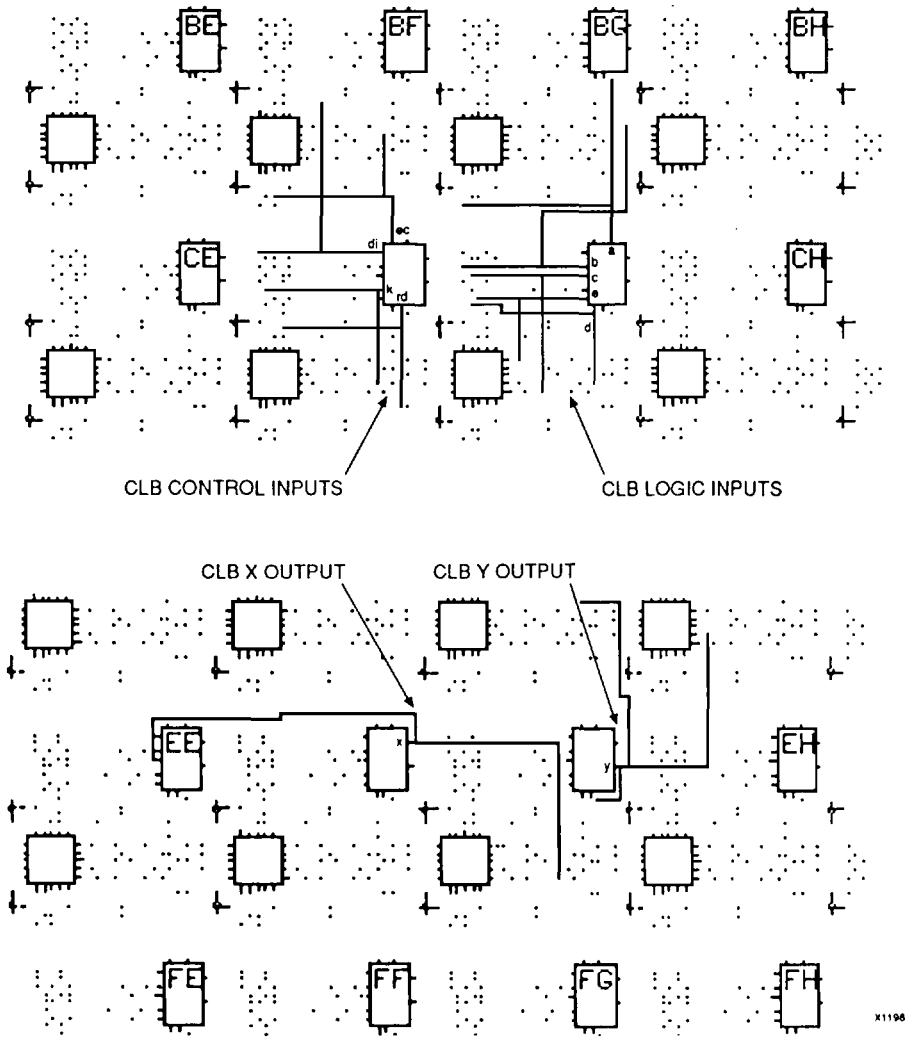


Figure 8. XACT Development System Locations of interconnect access, CLB control inputs, logic inputs and outputs. The dot pattern represents the available programmable interconnection points (PIPs).

Some of the interconnect PIPs are directional. This is indicated on the XACT design editor status line:

ND is a nondirectional interconnection.
D:H->V is a PIP that drives from a horizontal to a vertical line.
D:V->H is a PIP that drives from a vertical to a horizontal line.
D:C->T is a "T" PIP that drives from a cross of a T to the tail.
D:CW is a corner PIP that drives in the clockwise direction.
P0 indicates the PIP is non-conducting , P1 is on.

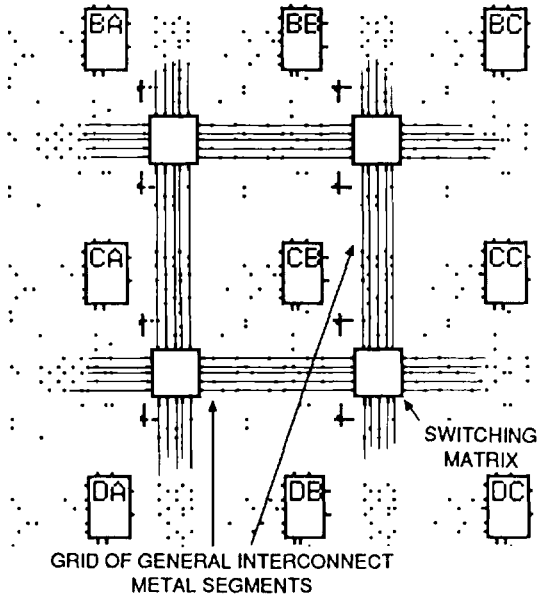


Figure 9. LCA General-Purpose Interconnect.
Composed of a grid of metal segments that may be interconnected through switch matrices to form networks for CLB and IOB inputs and outputs. X2664

Special buffers within the general interconnect areas provide periodic signal isolation and restoration for improved performance of lengthy nets. The interconnect buffers are available to propagate signals in either direction on a given general interconnect segment. These bidirectional (bidi) buffers are found adjacent to the switching matrices, above and to the right and may be highlighted by the use of the Show BIDI command in the XACT system. The other PIPs adjacent to the matrices are accessed to or from Longlines. The development system automatically defines the buffer direction based on the location of the interconnection network source. The delay calculator of the XACT development system automatically calculates and displays the block, interconnect and buffer delays for any paths selected. Generation of the simulation netlist with a worst-case delay model is provided by an XACT option.

Direct Interconnect

Direct interconnect, shown in Figure 11, provides the most efficient implementation of networks between adjacent CLBs or I/O Blocks. Signals routed from block to block using the direct interconnect exhibit minimum interconnect propagation and use no general interconnect resources. For each CLB, the X output may be connected directly to the B input of the CLB immediately to its right and to the C input of the CLB to its left. The Y output can use direct interconnect to drive the D input of the block immediately above and the A input of the block below. Direct intercon-

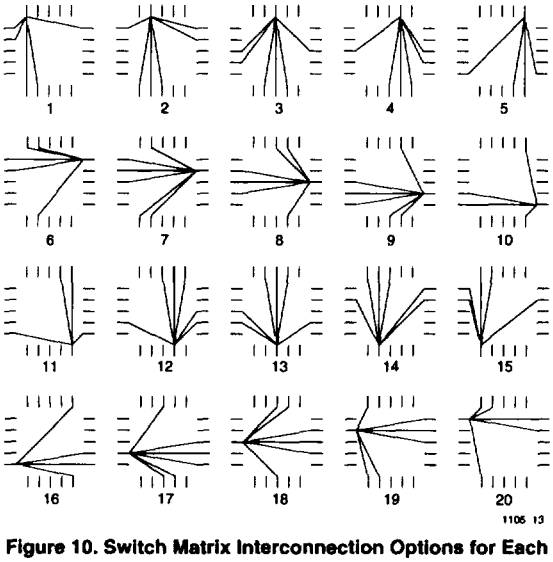


Figure 10. Switch Matrix Interconnection Options for Each Pin. Switch matrices on the edges are different. Use Show Matrix menu option in the XACT system

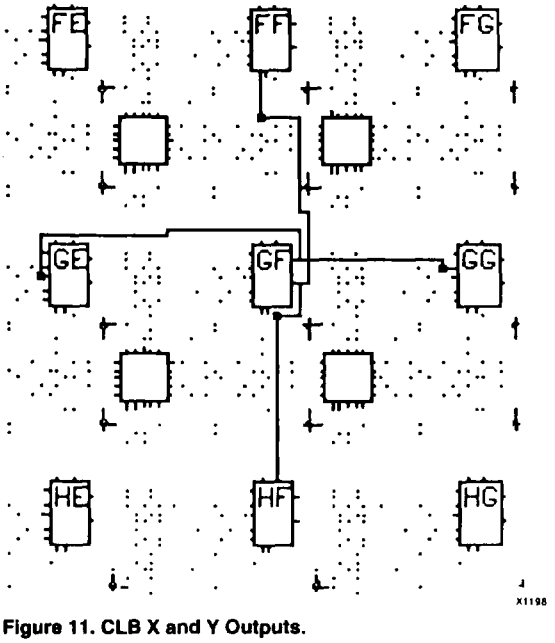


Figure 11. CLB X and Y Outputs.
The X and Y outputs of each CLB have single contact, direct access to inputs of adjacent CLBs

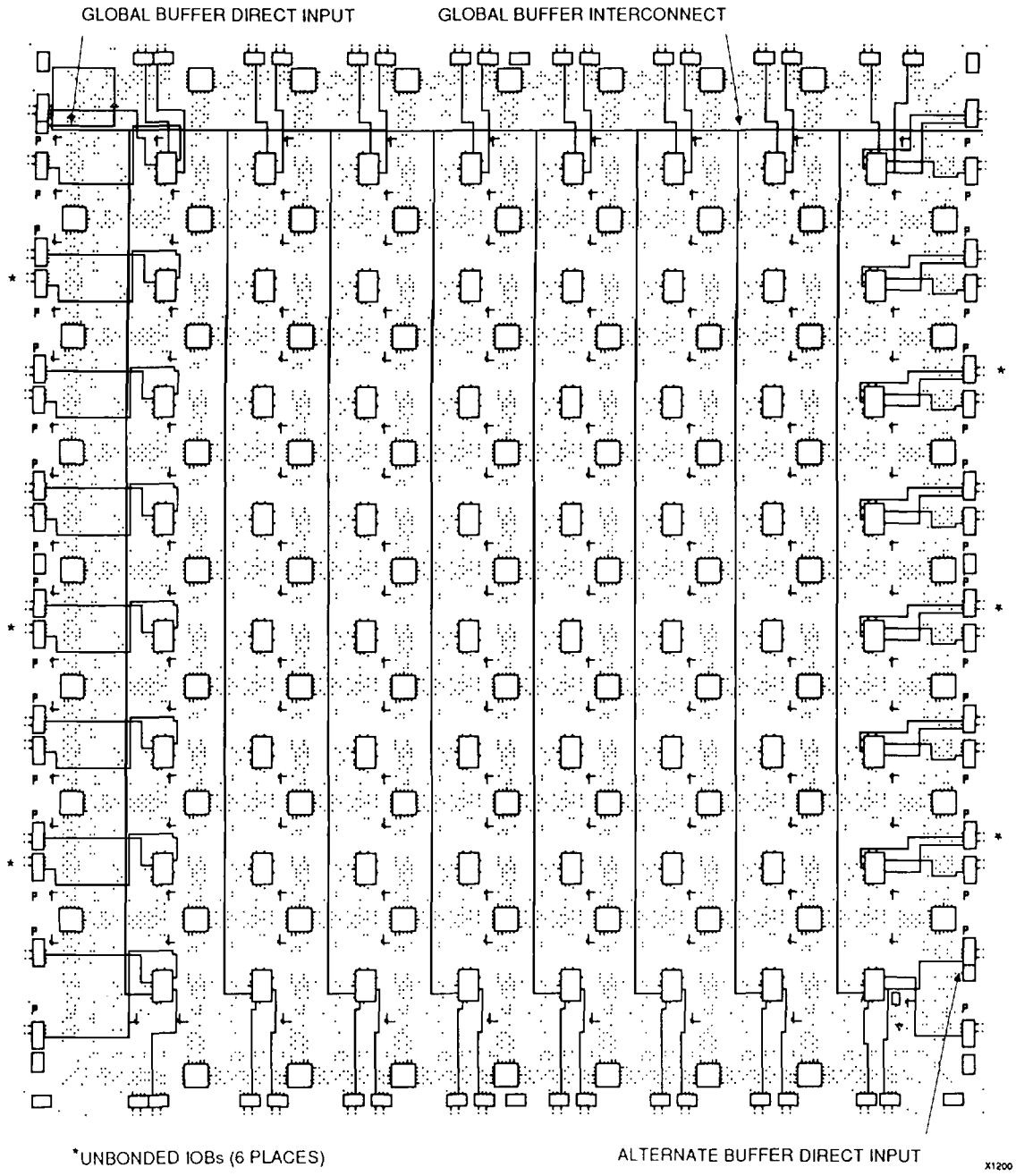


Figure 12. XC3020 Die-Edge IOBs. The XC3020 die-edge IOBs are provided with direct access to adjacent CLBs.

nect should be used to maximize the speed of high-performance portions of logic. Where logic blocks are adjacent to IOBs, direct connect is provided alternately to the IOB inputs (I) and outputs (O) on all four edges of the die. The right edge provides additional direct connects from CLB outputs to adjacent IOBs. Direct interconnections of IOBs with CLBs are shown in Figure 12.

Longlines

The Longlines bypass the switch matrices and are intended primarily for signals that must travel a long distance, or must have minimum skew among multiple destinations. Longlines, shown in Figure 13, run vertically and horizontally the height or width of the interconnect area. Each interconnection column has three vertical Longlines, and each interconnection row has two horizontal Longlines. Two additional Longlines are located adjacent to the outer sets of switching matrices. In devices larger than the XC3020, two vertical Longlines in each column are connectable half-length lines. On the XC3020, only the outer Longlines are connectable half-length lines.

Longlines can be driven by a logic block or IOB output on a column-by-column basis. This capability provides a common low skew control or clock line within each column of logic blocks. Interconnections of these Longlines are shown in Figure 14. Isolation buffers are provided at each input to a Longline and are enabled automatically by the development system when a connection is made.

A buffer in the upper left corner of the LCA chip drives a global net which is available to all K inputs of logic blocks. Using the global buffer for a clock signal provides a skew-free, high fan-out, synchronized clock for use at any or all of the IOBs and CLBs. Configuration bits for the K input to each logic block can select this global line or another routing resource as the clock source for its flip-flops. This net may also be programmed to drive the die edge clock lines for IOB use. An enhanced speed, CMOS threshold, direct access to this buffer is available at the second pad from the top of the left die edge.

A buffer in the lower right corner of the array drives a horizontal Longline that can drive programmed connections to a vertical Longline in each interconnection column. This alternate buffer also has low skew and high fan-out. The network formed by this alternate buffer's Longlines can be selected to drive the K inputs of the CLBs. CMOS threshold, high speed access to this buffer is available from the third pad from the bottom of the right die edge.

Internal Busses

A pair of 3-state buffers, located adjacent to each CLB, permits logic to drive the horizontal Longlines. Logic operation of the 3-state buffer controls allows them to implement wide multiplexing functions. Any 3-state buffer input can be selected as drive for the horizontal long-line bus by applying a Low logic level on its 3-state control line. See Figure 15a. The user is required to avoid contention which can result from multiple drivers with opposing logic

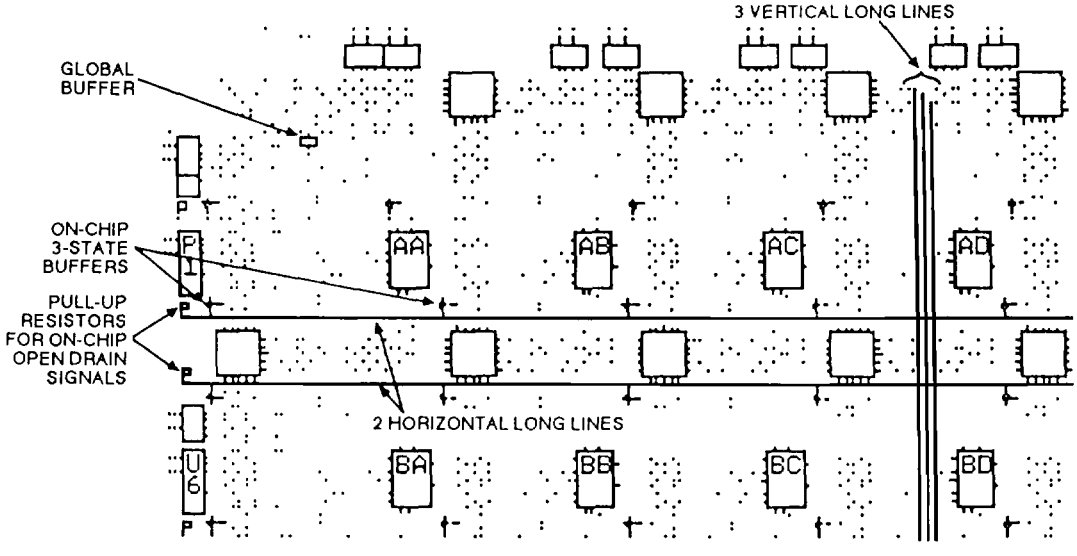


Figure 13. Horizontal and Vertical Longlines. These Longlines provide high fan-out, low-skew signal distribution in each row and column. The global buffer in the upper left die corner drives a common line throughout the LCA device.

levels. Control of the 3-state input by the same signal that drives the buffer input, creates an open-drain wired-AND function. A logic High on both buffer inputs creates a high impedance, which represents no contention. A logic Low enables the buffer to drive the Longline Low. See Figure 15b. Pull-up resistors are available at each end of the Longline to provide a High output when all connected buffers are non-conducting. This forms fast, wide gating functions. When data drives the inputs, and separate signals drive the 3-state control lines, these buffers form multiplexers (3-state busses). In this case, care must be used to prevent contention through multiple active buffers

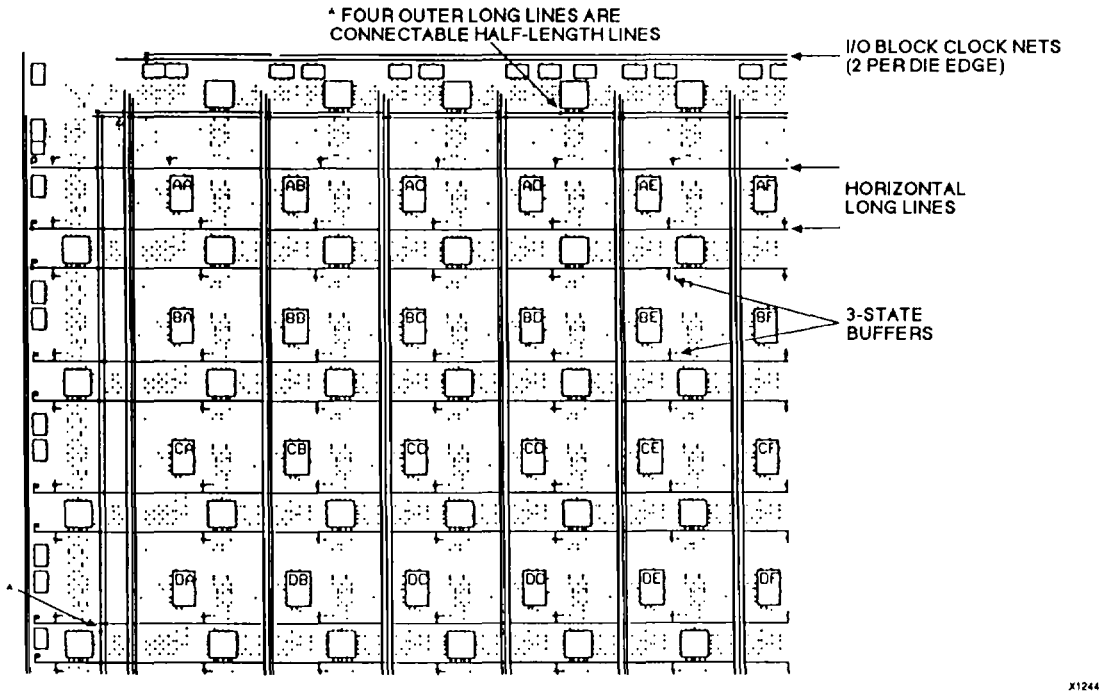


Figure 14. Programmable Interconnection of Longlines. This is provided at the edges of the routing area. Three-state buffers allow the use of horizontal Longlines to form on-chip wired AND and multiplexed buses. The left two non-clock vertical Longlines per column (except XC3020) and the outer perimeter Longlines may be programmed as connectible half-length lines.

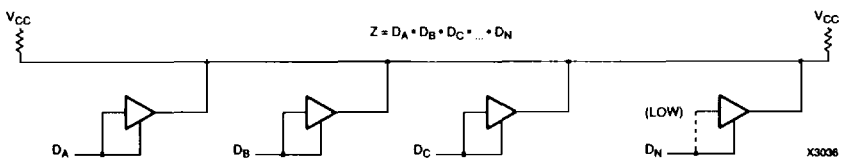
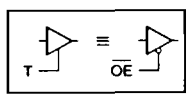


Figure 15a. 3-State Buffers Implement a Wired-AND Function. When all the buffer 3-state lines are High, (high impedance), the pull-up resistor(s) provide the High output. The buffer inputs are driven by the control signals or a Low.



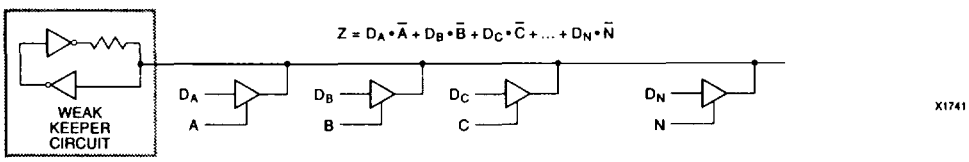


Figure 15b. 3-State Buffers Implement a Multiplexer. The selection is accomplished by the buffer 3-state signal.

of conflicting levels on a common line. Each horizontal Longline is also driven by a weak keeper circuit that prevents undefined floating levels by maintaining the previous logic level when the line is not driven by an active buffer or a pull-up resistor. Figure 16 shows 3-state buffers, Longlines and pull-up resistors.

Crystal Oscillator

Figure 16 also shows the location of an internal high speed inverting amplifier which may be used to implement an on-chip crystal oscillator. It is associated with the auxiliary buffer in the lower right corner of the die. When the oscillator is configured by MakeBits and connected as a signal source, two special user IOBs are also configured to connect the oscillator amplifier with external crystal oscillator components as shown in Figure 17. A divide by two option is available to assure symmetry. The oscillator circuit becomes active early in the configuration process to allow the oscillator to stabilize. Actual internal connection is delayed until completion of configuration. In Figure 17 the feedback resistor R1, between the output and input, biases the amplifier at threshold. The inversion of the amplifier, together with the R-C networks and an AT-cut series resonant crystal, produce the 360-degree phase shift of the Pierce oscillator. A series resistor R2 may be included to add to the amplifier output impedance when needed for phase-shift control, crystal resistance matching, or to limit the amplifier input swing to control clipping at large amplitudes. Excess feedback voltage may be corrected by the ratio of C2/C1. The amplifier is designed to be used from 1 MHz to about one-half the specified CLB toggle frequency. Use at frequencies below 1 MHz may require individual characterization with respect to a series

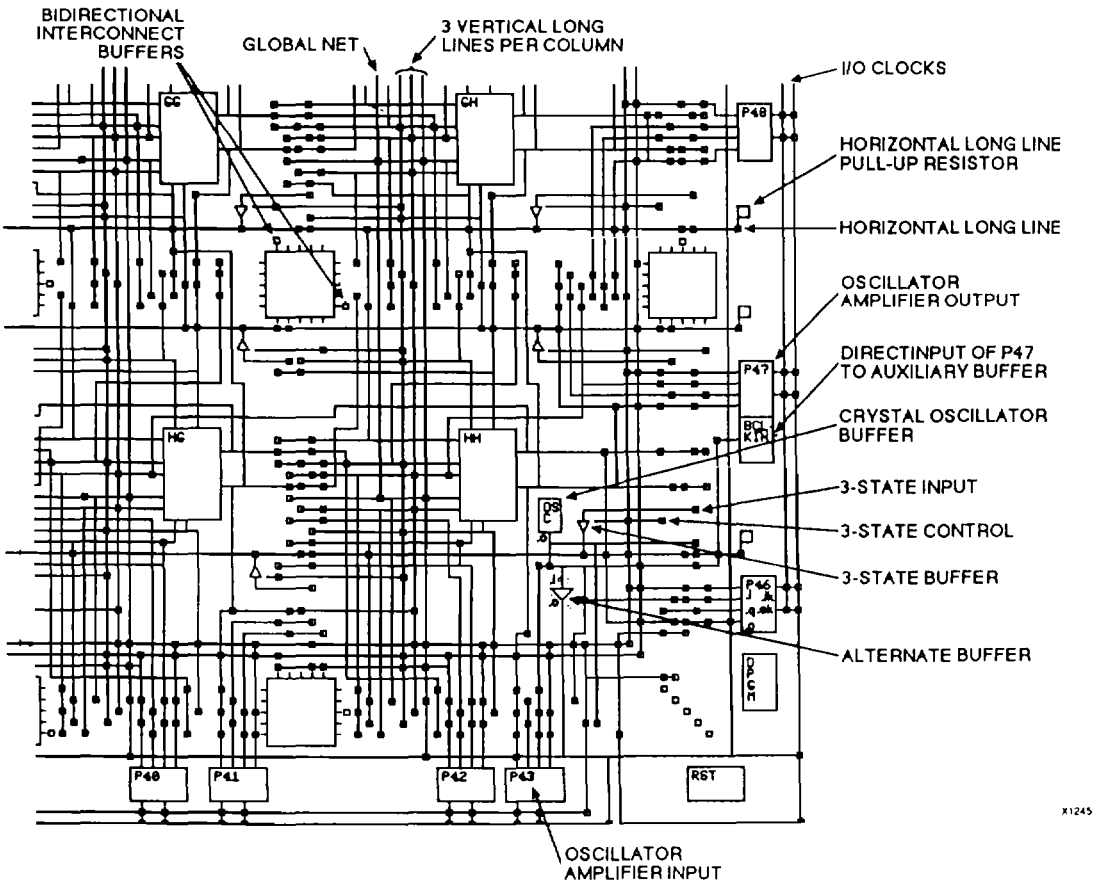
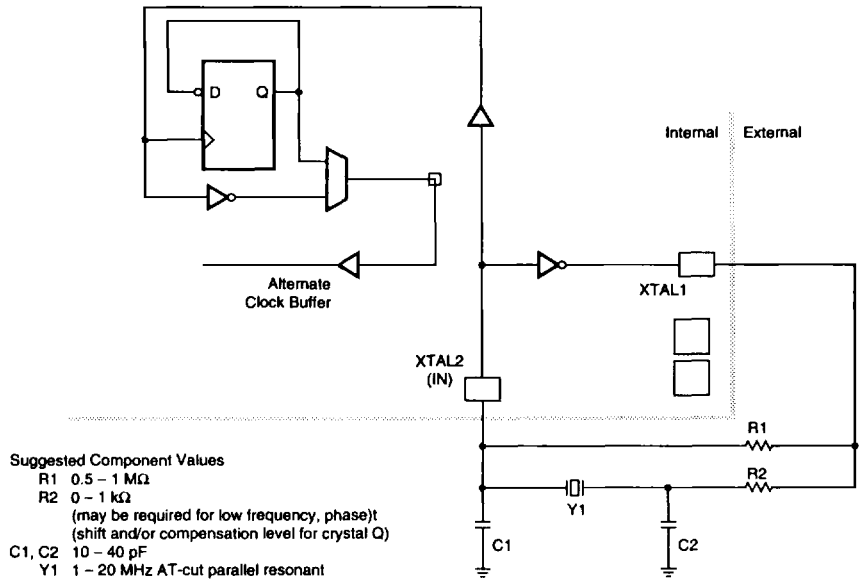


Figure 16. XACT Development System. An extra large view of possible interconnections in the lower right corner of the XC3020.



	44 PIN	68 PIN	84 PIN		100 PIN		132 PIN	160 PIN	164 PIN	175 PIN	208 PIN
	PLCC	PLCC	PLCC	PGA	CQFP	PQFP	PGA	PQFP	CQFP	PGA	PQFP
XTAL 1 (OUT)	30	47	57	J11	67	82	P13	82	105	T14	110
XTAL 2 (IN)	26	43	53	L11	61	76	M13	76	99	P15	100

X5302

Figure 17. Crystal Oscillator Inverter. When activated in the MakeBits program and by selecting an output network for its buffer, the crystal oscillator inverter uses two unconfigured package pins and external components to implement an oscillator. An optional divide-by-two mode is available to assure symmetry.

resistance. Crystal oscillators above 20 MHz generally require a crystal which operates in a third overtone mode, where the fundamental frequency must be suppressed by an inductor across C2, turning this parallel resonant circuit to double the fundamental crystal frequency, i.e., 2/3 of the desired third harmonic frequency network. When the oscillator inverter is not used, these IOBs and their package pins are available for general user I/O.

Programming

Table 1

M0	M1	M2	CCLK	Mode	Data
0	0	0	output	Master	Bit Serial
0	0	1	output	Master	Byte Wide Addr. = 0000 up
0	1	0	—	reserved	—
0	1	1	output	Master	Byte Wide Addr. = FFFF down
1	0	0	—	reserved	—
1	0	1	output	Peripheral	Byte Wide
1	1	0	—	reserved	—
1	1	1	input	Slave	Bit Serial

Initialization Phase

An internal power-on-reset circuit is triggered when power is applied. When Vcc reaches the voltage at which portions of the LCA device begin to operate (nominally 2.5 to 3 V), the programmable I/O output buffers are 3-stated and a high-impedance pull-up resistor is provided for the user I/O pins. A time-out delay is initiated to allow the power supply voltage to stabilize. During this time the power-down mode is inhibited. The Initialization state time-out (about 11 to 33 ms) is determined by a 14-bit counter driven by a self-generated internal timer. This nominal 1-MHz timer is subject to variations with process, temperature and power supply. As shown in Table 1, five configuration mode choices are available as determined by the input levels of three mode pins; M0, M1 and M2.

In Master configuration modes, the LCA device becomes the source of the Configuration Clock (CCLK). The beginning of configuration of devices using Peripheral or Slave modes must be delayed long enough for their initialization to be completed. An LCA device with mode lines selecting a Master configuration mode extends its initialization state using four times the delay (43 to 130 ms) to assure that all daisy-chained slave devices, which it may be driving, will

be ready even if the master is very fast, and the slave(s) very slow. Figure 18 shows the state sequences. At the end of Initialization, the LCA device enters the Clear state where it clears the configuration memory. The active Low, open-drain initialization signal $\overline{INIT}$ indicates when the Initialization and Clear states are complete. The LCA device tests for the absence of an external active Low $\overline{RESET}$ before it makes a final sample of the mode lines and enters the Configuration state. An external wired-AND of one or more $\overline{INIT}$ pins can be used to control configuration by the assertion of the active-Low $\overline{RESET}$ of a master mode device or to signal a processor that the LCA devices are not yet initialized.

If a configuration has begun, a re-assertion of $\overline{RESET}$ for a minimum of three internal timer cycles will be recognized and the LCA device will initiate an abort, returning to the Clear state to clear the partially loaded configuration memory words. The LCA device will then resample $\overline{RESET}$ and the mode lines before re-entering the Configuration state.

A re-program is initiated when a configured XC3000 family device senses a High-to-Low transition and subsequent >6 µs Low level on the Done/$\overline{PROG}$ package pin, or, if this pin is externally held permanently Low, a High-to-Low transition and subsequent >6 µs Low time on the $\overline{RESET}$ package pin.

The LCA device returns to the Clear state where the configuration memory is cleared and mode lines re-sampled, as for an aborted configuration. The complete configuration program is cleared and loaded during each configuration program cycle.

Length count control allows a system of multiple Logic Cell Arrays, of assorted sizes, to begin operation in a synchronized fashion. The configuration program generated by the MakePROM program of the XACT development system begins with a preamble of 111111110010 followed by a 24-bit length count representing the total number of configuration clocks needed to complete loading of the configuration program(s). The data framing is shown in Figure 19. All LCA devices connected in series read and shift preamble and length count in on positive and out on negative configuration clock edges. An LCA device which has received the preamble and length count then presents a High Data Out until it has intercepted the appropriate number of data frames. When the configuration program memory of an LCA device is full and the length count does not yet compare, the LCA device shifts any additional data through, as it did for preamble and length count.

When the LCA device configuration memory is full and the length count compares, the LCA device will execute a synchronous start-up sequence and become operational. See Figure 20. Two CCLK cycles after the completion of loading configuration data, the user I/O pins are enabled as configured. As selected in MakeBits, the internal user-logic RESET is released either one clock cycle before or after the I/O pins become active. A similar timing selection is programmable for the DONE/$\overline{PROG}$ output signal. DONE/$\overline{PROG}$ may also be programmed to be an open drain or include a pull-up resistor to accommodate wired ANDing. The High During Configuration (HDC) and Low During Configuration ($\overline{LDC}$) are two user I/O pins which are driven active while an LCA device is in its Initialization,

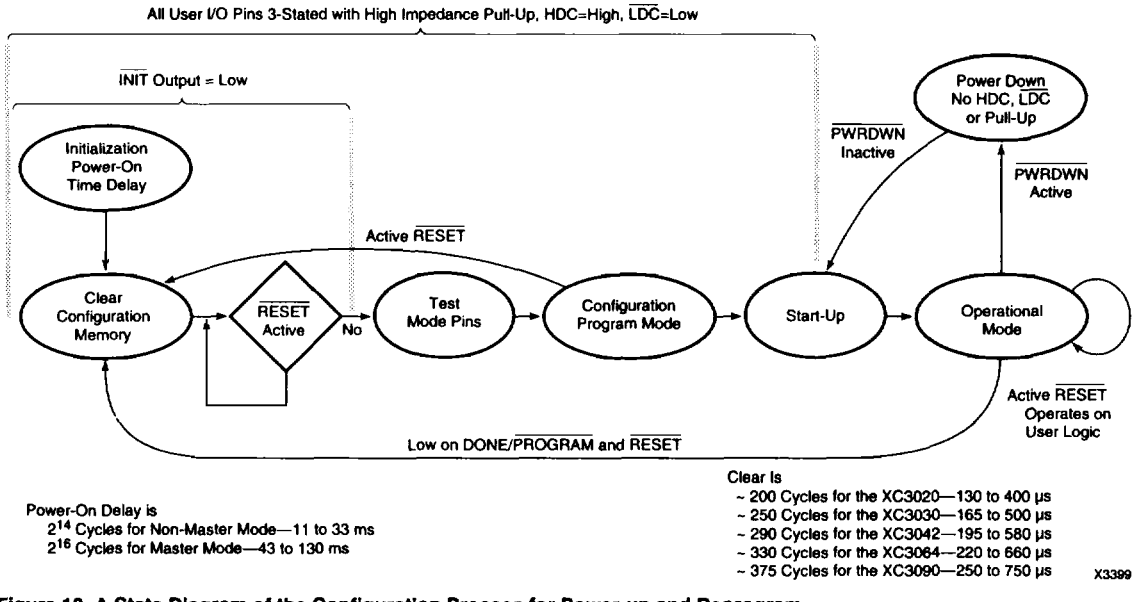


Figure 18. A State Diagram of the Configuration Process for Power-up and Reprogram.

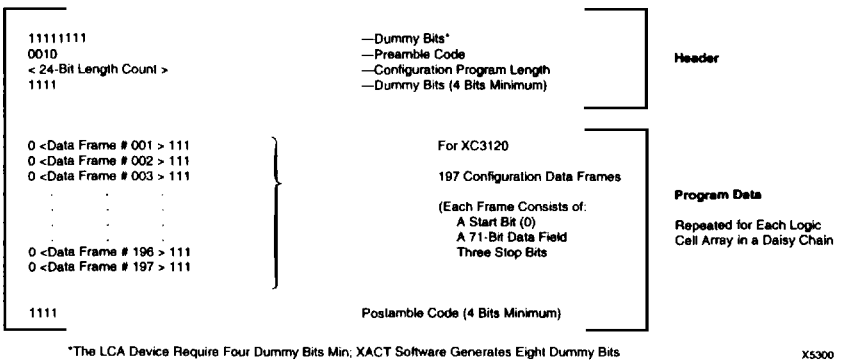
Clear or Configure states. They and DONE/PROG provide signals for control of external logic signals such as RESET, bus enable or PROM enable during configuration. For parallel Master configuration modes, these signals provide PROM enable control and allow the data pins to be shared with user logic signals.

User I/O inputs can be programmed to be either TTL or CMOS compatible thresholds. At power-up, all inputs have TTL thresholds and can change to CMOS thresholds at the completion of configuration if the user has selected CMOS thresholds. The threshold of PWRDWN and the direct clock inputs are fixed at a CMOS level.

If the crystal oscillator is used, it will begin operation before configuration is complete to allow time for stabilization before it is connected to the internal circuitry.

Configuration Data

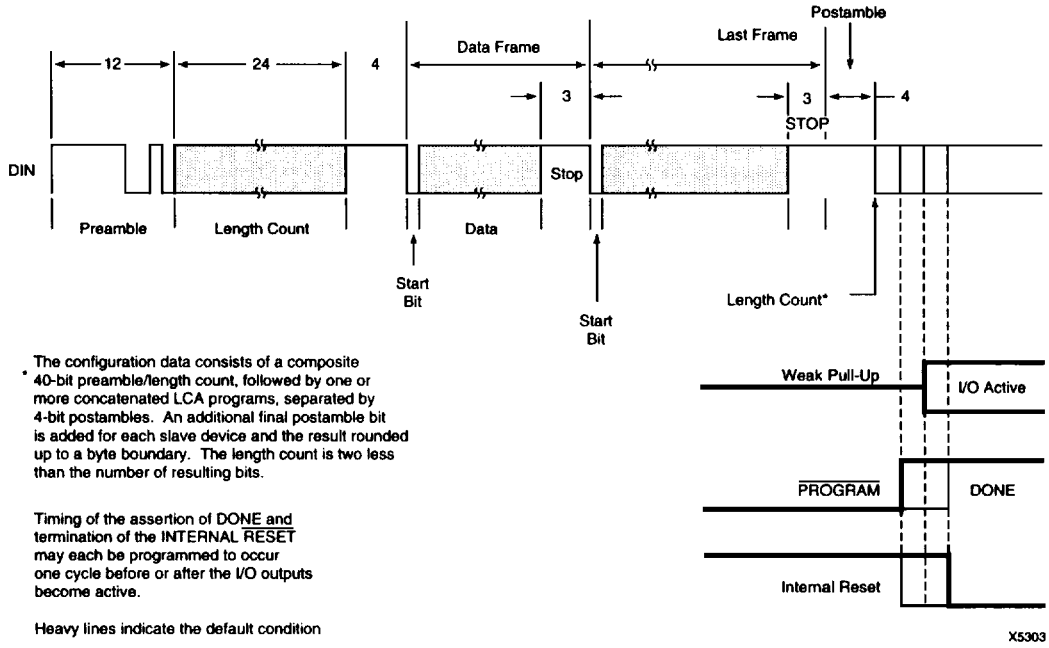
Configuration data to define the function and interconnection within a Logic Cell Array is loaded from an external



Device	XC3020 XC3020A XC3020L XC3120 XC3120A	XC3030 XC3030A XC3030L XC3130 XC3130A	XC3042 XC3042A XC3042L XC3142 XC3142A	XC3064 XC3064A XC3064L XC3164 XC3164A	XC3090 XC3090A XC3090L XC3190 XC3190A	XC3195 XC3195A
Gates	1,000 to 1,500	1,500 to 2,000	2,000 to 3,000	3,500 to 4,500	5,000 to 6,000	6,500 to 7,500
CLBs Row x Col	64 (8 x 8)	100 (10 x 10)	144 (12 x 12)	224 (16 x 14)	320 (20 x 16)	484 (22 x 22)
IOBs	64	80	96	120	144	176
Flip-flops	256	360	480	688	928	1,320
Horizontal Longlines	16	20	24	32	40	44
TBUFs/Horizontal LL	9	11	13	15	17	23
Bits per Frame (including1 start and 3 stop bits)	75	92	108	140	172	188
Frames	197	241	285	329	373	505
Program Data = Bits x Frames + 4 bits (excludes header)	14,779	22,176	30,784	46,064	64,160	94,944
PROM size (bits) = Program Data + 40-bit Header	14,819	22,216	30,824	46,104	64,200	94,984

Figure 19. Internal Configuration Data Structure for an LCA Device. This shows the preamble, length count and data frames generated by the XACT Development System.

The Length Count produced by the MakeBits program = [(40-bit preamble + sum of program data + 1 per daisy chain device) rounded up to multiple of 8] – (2 ≤ K ≤ 4) where K is a function of DONE and RESET timing selected. An additional 8 is added if roundup increment is less than K. K additional clocks are needed to complete start-up after length count is reached.



* The configuration data consists of a composite 40-bit preamble/length count, followed by one or more concatenated LCA programs, separated by 4-bit postambles. An additional final postamble bit is added for each slave device and the result rounded up to a byte boundary. The length count is two less than the number of resulting bits.

Timing of the assertion of DONE and termination of the INTERNAL $\overline{\text{RESET}}$ may each be programmed to occur one cycle before or after the I/O outputs become active.

Heavy lines indicate the default condition

Figure 20. Configuration and Start-up of One or More LCA Devices.

storage at power-up and after a re-program signal. Several methods of automatic and controlled loading of the required data are available. Logic levels applied to mode selection pins at the start of configuration time determine the method to be used. See Table 1. The data may be either bit-serial or byte-parallel, depending on the configuration mode. The different LCA devices have different sizes and numbers of data frames. To maintain compatibility between various device types, the Xilinx product families use compatible configuration formats. For the XC3020, configuration requires 14779 bits for each device, arranged in 197 data frames. An additional 40 bits are used in the header. See Figure 20. The specific data format for each device is produced by the MakeBits command of the development system and one or more of these files can then be combined and appended to a length count preamble and be transformed into a PROM format file by the MakePROM command of the XACT development system. A compatibility exception precludes the use of an XC2000-series device as the master for XC3000-series devices if their DONE or RESET are programmed to occur after their outputs become active.

The Tie Option of the MakeBits program defines output levels of unused blocks of a design and connects these to unused routing resources. This prevents indeterminate levels that might produce parasitic supply currents. If unused blocks are not sufficient to complete the tie, the Flagnet command of EDITLCA can be used to indicate nets which must not be used to drive the remaining unused routing, as that might affect timing of user nets. Norestore will retain the results of tie for timing analysis with Querynet before Restore returns the design to the untied condition. Tie can be omitted for quick breadboard iterations where a few additional milliamps of I_{CC} are acceptable.

The configuration bitstream begins with eight High preamble bits, a 4-bit preamble code and a 24-bit length count. When configuration is initiated, a counter in the LCA device is set to zero and begins to count the total number of configuration clock cycles applied to the device. As each configuration data frame is supplied to the LCA device, it is internally assembled into a data word, which is then loaded in parallel into one word of the internal configuration memory array. The configuration loading process is complete when the current length count equals the loaded length count and the required configuration program data frames have been written. Internal user flip-flops are held Reset during configuration.

Two user-programmable pins are defined in the unconfigured Logic Cell array. High During Configuration (HDC) and Low During Configuration ($\overline{\text{LDC}}$) as well as DONE/$\overline{\text{PROG}}$ may be used as external control signals during configuration. In Master mode configurations it is convenient to use $\overline{\text{LDC}}$ as an active-Low EPROM Chip

Enable. After the last configuration data bit is loaded and the length count compares, the user I/O pins become active. Options in the MakeBits program allow timing choices of one clock earlier or later for the timing of the end of the internal logic RESET and the assertion of the DONE signal. The open-drain DONE/PROG output can be AND-tied with multiple LCA devices and used as an active-High READY, an active-Low PROM enable or a RESET to other portions of the system. The state diagram of Figure 18 illustrates the configuration process.

Master Mode

In Master mode, the LCA device automatically loads configuration data from an external memory device. There are three Master modes that use the internal timing source to supply the configuration clock (CCLK) to time the incoming data. Master Serial mode uses serial configuration data supplied to Data-in (DIN) from a synchronous serial source such as the Xilinx Serial Configuration PROM shown in Figure 21. Master Parallel Low and High modes automatically use parallel data supplied to the D0–D7 pins in response to the 16-bit address generated by the LCA device. Figure 22 shows an example of the parallel Master mode connections required. The LCA HEX starting address is 0000 and increments for Master Low mode and it is FFFF and decrements for Master High mode. These two modes provide address compatibility with microprocessors which begin execution from opposite ends of memory.

Peripheral Mode

Peripheral mode provides a simplified interface through which the device may be loaded byte-wide, as a processor peripheral. Figure 23 shows the peripheral mode connections. Processor write cycles are decoded from the common assertion of the active low Write Strobe ($\overline{WS}$), and two active low and one active high Chip Selects ($\overline{CS0}$, $\overline{CS1}$, CS2). The LCA device generates a configuration clock from the internal timing generator and serializes the parallel input data for internal framing or for succeeding slaves on Data Out (DOUT). A output High on READY/$\overline{BUSY}$ pin indicates the completion of loading for each byte when the input register is ready for a new byte. As with Master modes, Peripheral mode may also be used as a lead device for a daisy-chain of slave devices.

Slave Serial Mode

Slave Serial mode provides a simple interface for loading the Logic Cell Array configuration as shown in Figure 24. Serial data is supplied in conjunction with a synchronizing input clock. Most Slave mode applications are in daisy-chain configurations in which the data input is driven from the previous Logic Cell Array's data out, while the clock is supplied by a lead device in Master or Peripheral mode. Data may also be supplied by a processor or other special circuits.

Daisy Chain

The XACT development system is used to create a composite configuration for selected LCA devices including: a preamble, a length count for the total bitstream, multiple concatenated data programs and a postamble plus an additional fill bit per device in the serial chain. After loading and passing-on the preamble and length count to a possible daisy-chain, a lead device will load its configuration data frames while providing a High DOUT to possible down-stream devices as shown in Figure 22. Loading continues while the lead device has received its configuration program and the current length count has not reached the full value. The additional data is passed through the lead device and appears on the Data Out (DOUT) pin in serial form. The lead device also generates the Configuration Clock (CCLK) to synchronize the serial output data and data in of down-stream LCA devices. Data is read in on DIN of slave devices by the positive edge of CCLK and shifted out the DOUT on the negative edge of CCLK. A parallel Master mode device uses its internal timing generator to produce an internal CCLK of 8 times its EPROM address rate, while a Peripheral mode device produces a burst of 8 CCLKs for each chip select and write-strobe cycle. The internal timing generator continues to operate for general timing and synchronization of inputs in all modes.

Special Configuration Functions

The configuration data includes control over several special functions in addition to the normal user logic functions and interconnect.

- Input thresholds
- Readback disable
- DONE pull-up resistor
- DONE timing
- RESET timing
- Oscillator frequency divided by two

Each of these functions is controlled by configuration data bits which are selected as part of the normal XACT development system bitstream generation process.

Input Thresholds

Prior to the completion of configuration all LCA device input thresholds are TTL compatible. Upon completion of configuration, the input thresholds become either TTL or CMOS compatible as programmed. The use of the TTL threshold option requires some additional supply current for threshold shifting. The exception is the threshold of the $\overline{PWRDWN}$ input and direct clocks which always have a CMOS input. Prior to the completion of configuration the user I/O pins each have a high impedance pull-up. The

configuration program can be used to enable the IOB pull-up resistors in the Operational mode to act either as an input load or to avoid a floating input on an otherwise unused pin.

Readback

The contents of a Logic Cell Array may be read back if it has been programmed with a bitstream in which the Readback option has been enabled. Readback may be used for verification of configuration and as a method of determining the state of internal logic nodes during debugging. There are three options in generating the configuration bitstream.

- "Never" inhibits the Readback capability.
- "One-time," inhibits Readback after one Readback has been executed to verify the configuration.
- "On-command" allows unrestricted use of Readback.

Readback is accomplished without the use of any of the user I/O pins; only M0, M1 and CCLK are used. The initiation of Readback is produced by a Low to High transition of the M0/RTRIG (Read Trigger) pin. The CCLK input must then be driven by external logic to read back the configuration data. The first three Low-to-High CCLK transitions clock out dummy data. The subsequent Low-to-High CCLK transitions shift the data frame information out on the M1/$\overline{\text{RDATA}}$ (Read Data) pin. Note that the logic polarity is always inverted, a zero in configuration becomes a one in Readback, and vice versa. Note also that each Readback frame has one Start bit (read back as a one) but, unlike in configuration, each Readback frame has only one Stop bit (read back as a zero). The third leading dummy bit mentioned above can be considered the Start bit of the first frame. All data frames must be read back to complete the process and return the Mode Select and CCLK pins to their normal functions.

Readback data includes the current state of each CLB flip-flop, each input flip-flop or latch, and each device pad. These data are imbedded into unused configuration bit positions during Readback. This state information is used by the XACT development system In-Circuit Verifier to provide visibility into the internal operation of the logic while the system is operating. To readback a uniform time-sample of all storage elements, it may be necessary to inhibit the system clock.

Reprogram

To initiate a re-programming cycle, the dual-function pin DONE/$\overline{\text{PROG}}$ must be given a High-to-Low transition. To reduce sensitivity to noise, the input signal is filtered for two cycles of the LCA device internal timing generator. When reprogram begins, the user-programmable I/O output buffers are disabled and high-impedance pull-ups are provided for the package pins. The device returns to the Clear state and clears the configuration memory before it indicates 'initialized'. Since this Clear operation uses chip-individual internal timing, the master might complete the Clear operation and then start configuration before the slave has completed the Clear operation. To avoid this problem, the slave $\overline{\text{INIT}}$ pins must be AND-wired and used to force a $\overline{\text{RESET}}$ on the master (see Figure 22). Reprogram control is often implemented using an external open-collector driver which pulls DONE/$\overline{\text{PROG}}$ Low. Once a stable request is recognized, the DONE/$\overline{\text{PROG}}$ pin is held Low until the new configuration has been completed. Even if the re-program request is externally held Low beyond the configuration period, the LCA device will begin operation upon completion of configuration.

DONE Pull-up

DONE/$\overline{\text{PROG}}$ is an open-drain I/O pin that indicates the LCA device is in the operational state. An optional internal pull-up resistor can be enabled by the user of the XACT development system when MAKEBITS is executed. The DONE/$\overline{\text{PROG}}$ pins of multiple LCA devices in a daisy-chain may be connected together to indicate all are DONE or to direct them all to reprogram.

DONE Timing

The timing of the DONE status signal can be controlled by a selection in the MakeBits program to occur either a CCLK cycle before, or after, the outputs going active. See Figure 20. This facilitates control of external functions such as a PROM enable or holding a system in a wait state.

RESET Timing

As with DONE timing, the timing of the release of the internal reset can be controlled by a selection in the MakeBits program to occur either a CCLK cycle before, or after, the outputs going active. See Figure 20. This reset keeps all user programmable flip-flops and latches in a zero state during configuration.

Crystal Oscillator Division

A selection in the MakeBits program allows the user to incorporate a dedicated divide-by-two flip-flop between the crystal oscillator and the alternate clock line. This guarantees a symmetrical clock signal. Although the frequency stability of a crystal oscillator is very good, the symmetry of its waveform can be affected by bias or feedback drive.

The following seven pages describe the different configuration modes in detail

Master Serial Mode

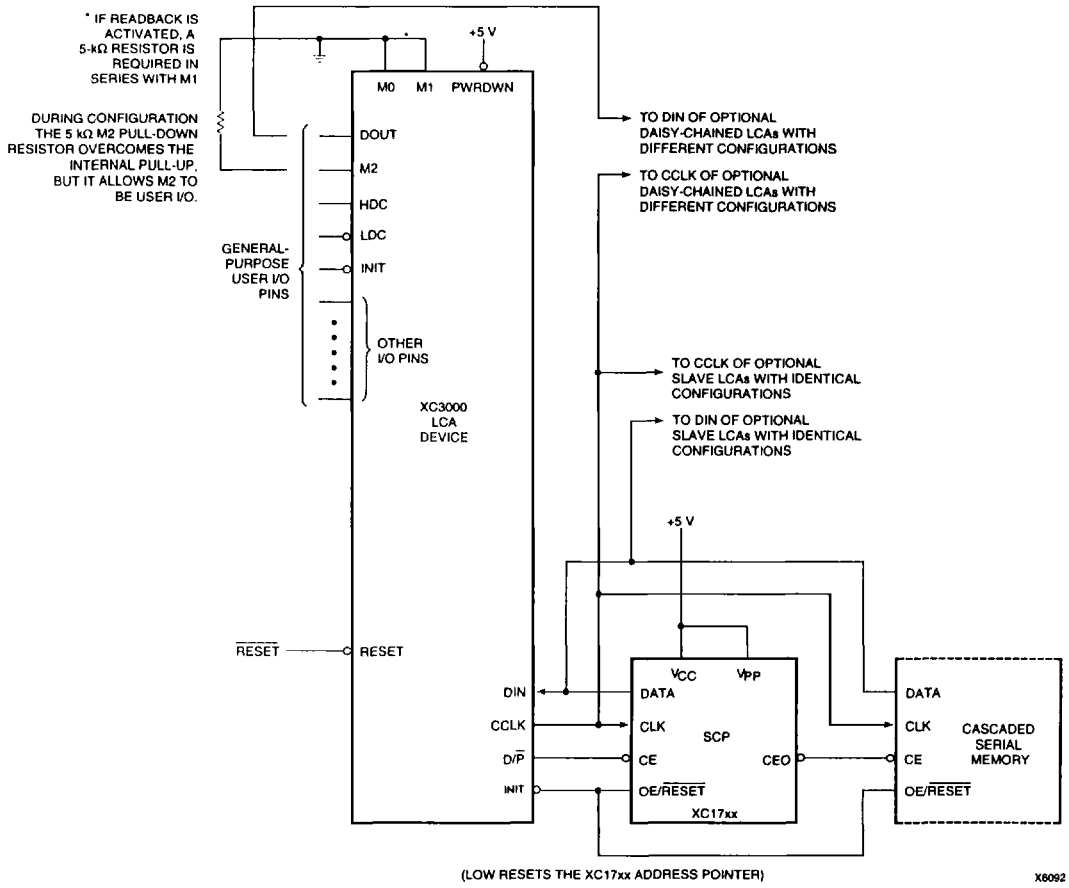


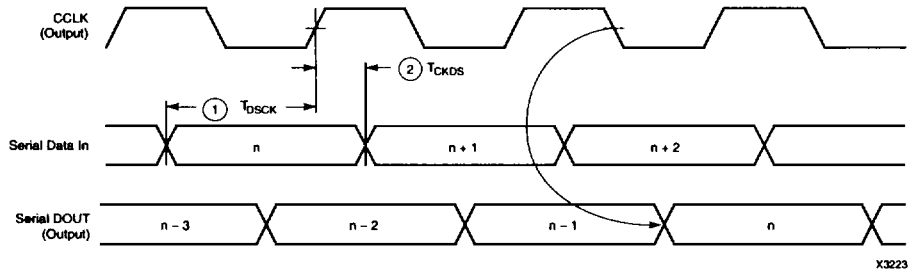
Figure 21. Master Serial Mode

In Master Serial mode, the CCLK output of the lead LCA device drives a Xilinx Serial PROM that feeds the LCA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. This puts the next data bit on the SPROM data output, connected to the LCA DIN pin. The lead LCA device accepts this data on the subsequent rising CCLK edge.

The lead LCA device then presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next LCA device in the daisy-chain accepts data on the subsequent rising CCLK edge.

The SPROM CE input can be driven from either $\overline{LDC}$ or DONE . Using $\overline{LDC}$ avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but $\overline{LDC}$ is then restricted to be a permanently High user output. Using DONE also avoids contention on DIN, provided the early DONE option is invoked.

Master Serial Mode Programming Switching Characteristics



	Speed Grade		Min	Max	Units
	Description	Symbol			
CCLK	Data In setup	1 T_{DSCK}	60		ns
	Data In hold	2 $_{CKDS}$	0		ns

Notes:
1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until V_{CC} has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require >6-µs High level on RESET, followed by a >6-µs Low level on $\overline{\text{RESET}}$ and D/$\overline{\text{P}}$ after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).
2. Configuration can be controlled by holding $\overline{\text{RESET}}$ Low with or until after the $\overline{\text{INIT}}$ of all daisy-chain slave-mode devices is High.
3. Master-serial-mode timing is based on slave-mode testing.

Master Parallel Mode

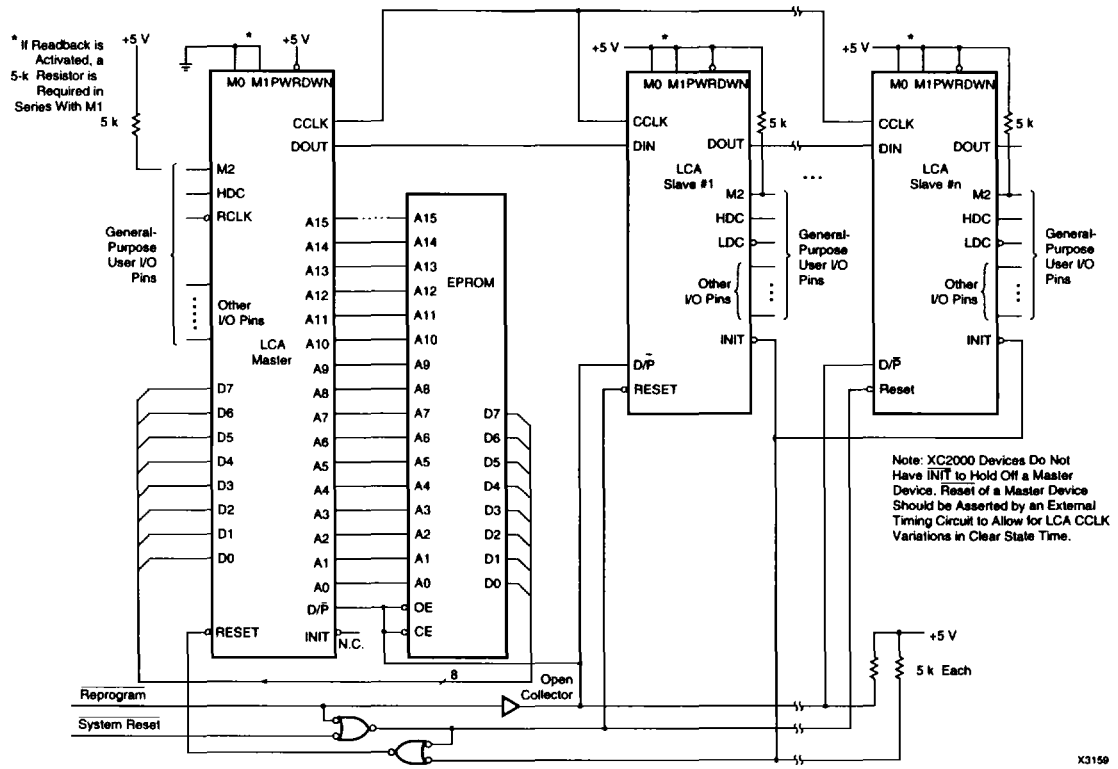
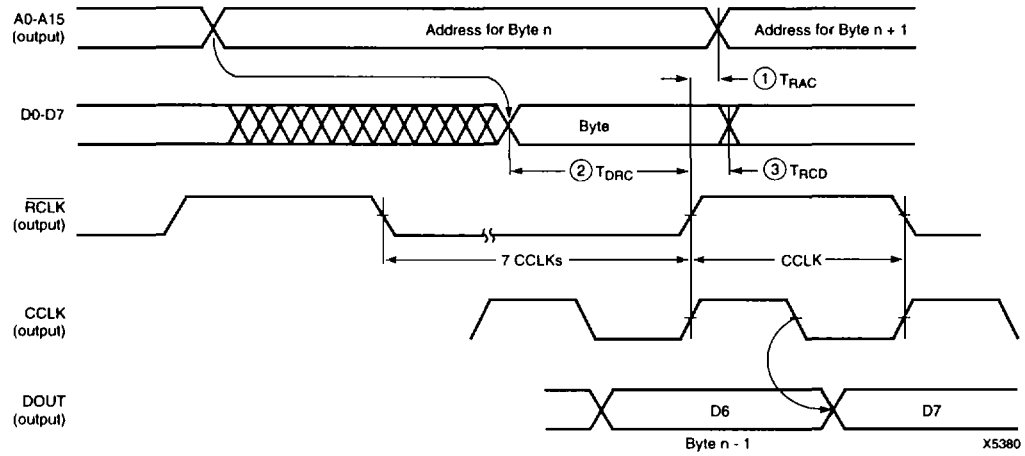


Figure 22. Master Parallel Mode

In Master Parallel mode, the lead LCA device directly addresses an industry-standard byte-wide EPROM and accepts eight data bits right before incrementing (or decrementing) the address outputs.

The eight data bits are serialized in the lead LCA device, which then presents the preamble data (and all data that overflows the lead device) on the DOUT pin. There is an internal delay of 1.5 CCLK periods, after the rising CCLK edge that accepts a byte of data, and also changes the EPROM address, until the falling CCLK edge that makes the LSB (D0) of this byte appear at DOUT. This means that DOUT changes on the falling CCLK edge, and the next LCA device in the daisy chain accepts data on the subsequent rising CCLK edge.

Master Parallel Mode Programming Switching Characteristics



	Description	Symbol		Min	Max	Units
RCLK	To address valid	1	T_{RAC}	0	200	ns
	To data setup	2	T_{DRC}	60		ns
	To data hold	3	T_{RCD}	0		ns
	RCLK High		T_{RCH}	600		ns
	RCLK Low		T_{RCL}	4.0		µs

Notes: 1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until V_{CC} has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6-µs High level on RESET, followed by a >6-µs Low level on RESET and D/P after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).
2. Configuration can be controlled by holding RESET Low with or until after the INIT of all daisy-chain slave-mode devices is High.

This timing diagram shows that the EPROM requirements are extremely relaxed:
EPROM access time can be longer than 4000 ns. EPROM data output has no hold time requirements.

Peripheral Mode

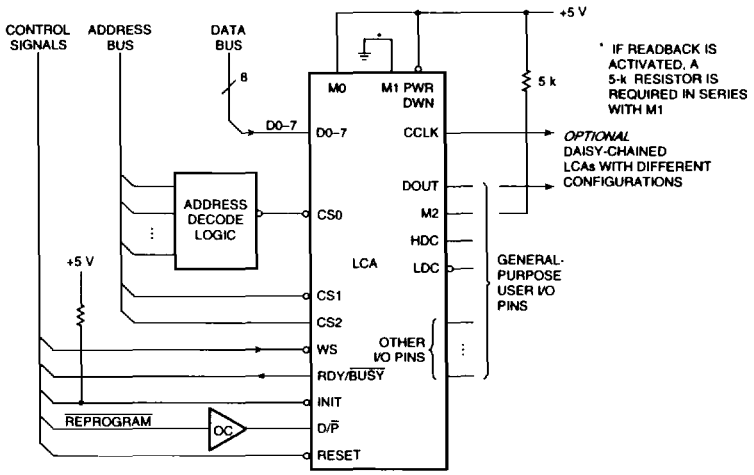


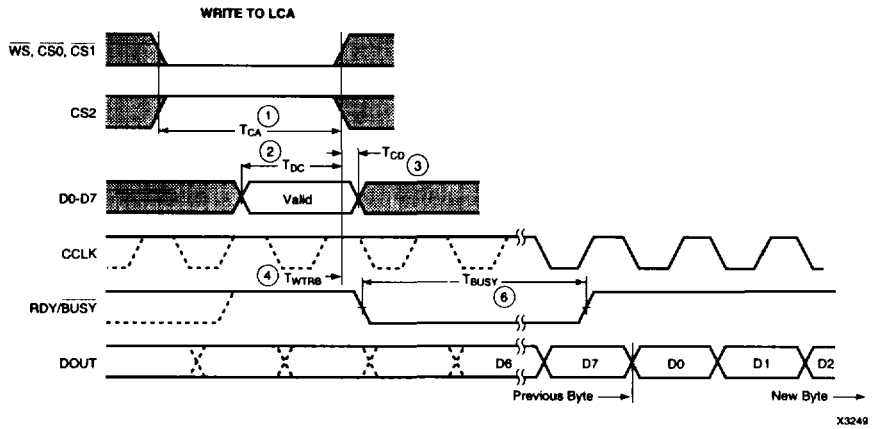
Figure 23. Peripheral Mode.

Peripheral mode uses the trailing edge of the logic AND condition of the $\overline{CS0}$, $\overline{CS1}$, CS2, and $\overline{WS}$ inputs to accept byte-wide data from a microprocessor bus. In the lead LCA device, this data is loaded into a double-buffered UART-like parallel-to-serial converter and is serially shifted into the internal logic. The lead LCA device presents the preamble data (and all data that overflows the lead device) on the DOUT pin.

The Ready/Busy output from the lead LCA device acts as a handshake signal to the microprocessor. RDY/$\overline{BUSY}$ goes Low when a byte has been received, and goes High again when the byte-wide input buffer has transferred its information into the shift register, and the buffer is ready to receive new data. The length of the $\overline{BUSY}$ signal depends on the activity in the UART. If the shift register had been empty when the new byte was received, the $\overline{BUSY}$ signal lasts for only two CCLK periods. If the shift register was still full when the new byte was received, the $\overline{BUSY}$ signal can be as long as nine CCLK periods.

Note that after the last byte has been entered, only seven of its bits are shifted out. CCLK remains High with DOUT equal to bit 6 (the next-to-last bit) of the last byte entered.

Peripheral Mode Programming Switching Characteristics



	Description	Symbol		Min	Max	Units
Write	Effective Write time required (Assertion of $\overline{CS0}$, $\overline{CS1}$, CS2, $\overline{WS}$)	1	T_{CA}	100		ns
	DIN Setup time required	2	T_{DC}	60		ns
	DIN Hold time required	3	T_{CD}	0		ns
	RDY/$\overline{BUSY}$ delay after end of $\overline{WS}$	4	T_{WTRB}		60	ns
RDY	Earliest next $\overline{WS}$ after end of $\overline{BUSY}$	5	T_{RBWT}	0		ns
	$\overline{BUSY}$ Low time generated	6	T_{BUSY}	2.5	9	CCLK Periods

Notes:

1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding $\overline{RESET}$ Low until V_{CC} has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6-µs High level on $\overline{RESET}$, followed by a >6-µs Low level on $\overline{RESET}$ and D/$\overline{P}$ after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).
2. Configuration must be delayed until the $\overline{INIT}$ of all LCAs is High.
3. Time from end of $\overline{WS}$ to CCLK cycle for the new byte of data depends on completion of previous byte processing and the phase of the internal timing generator for CCLK.
4. CCLK and DOUT timing is tested in slave mode.
5. T_{BUSY} indicates that the double-buffered parallel-to-serial converter is not yet ready to receive new data. The shortest T_{BUSY} occurs when a byte is loaded into an empty parallel-to-serial converter. The longest T_{BUSY} occurs when a new word is loaded into the input register before the second-level buffer has started shifting out data.

This timing diagram shows very relaxed requirements: Data need not be held beyond the rising edge of $\overline{WS}$. $\overline{BUSY}$ will go active within 60 ns after the end of $\overline{WS}$. $\overline{BUSY}$ will stay active for several microseconds. $\overline{WS}$ may be asserted immediately after the end of $\overline{BUSY}$.

Slave Serial Mode

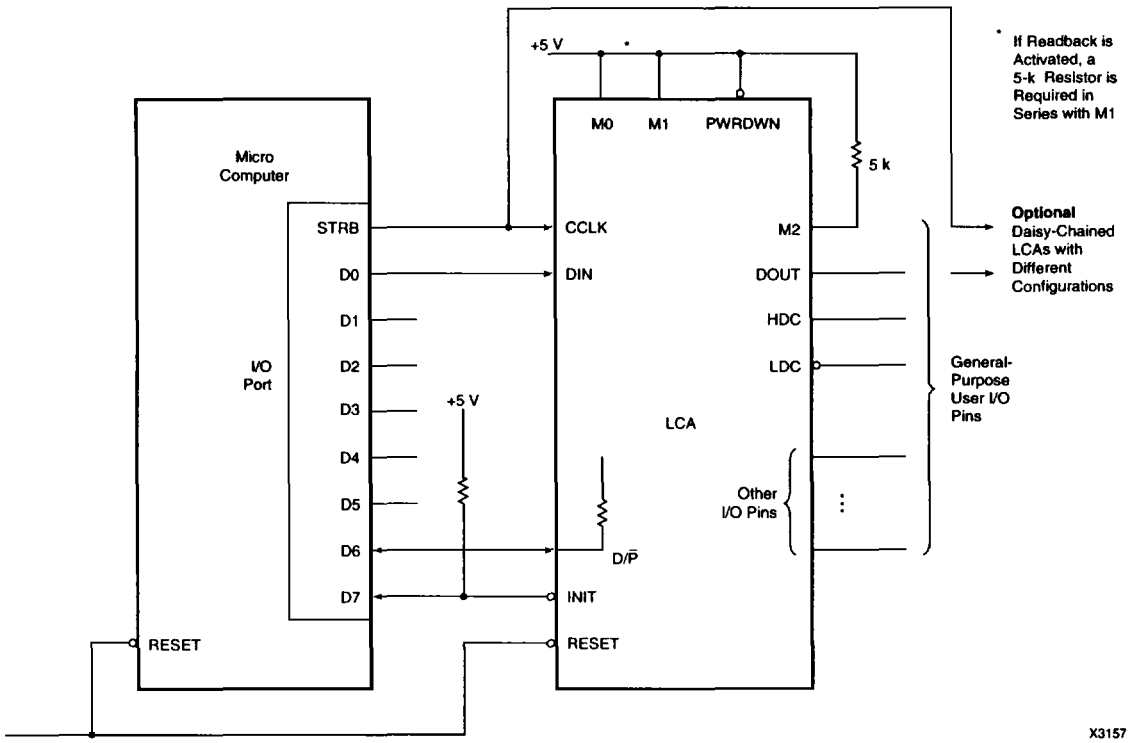
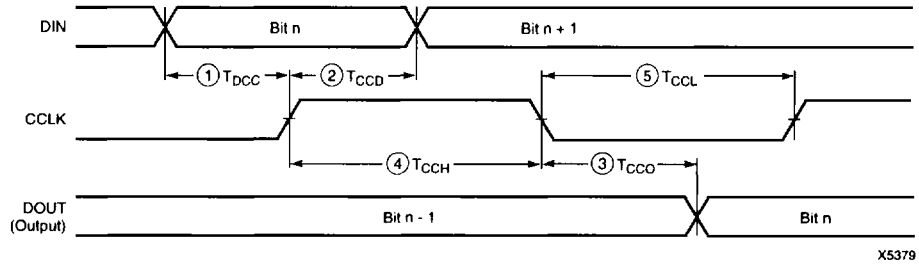


Figure 24. Slave Serial Mode.

In Slave Serial mode, an external signal drives the CCLK input(s) of the LCA device(s). The serial configuration bitstream must be available at the DIN input of the lead LCA device a short set-up time before each rising CCLK edge. The lead LCA device then presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next LCA device in the daisy-chain accepts data on the subsequent rising CCLK edge.

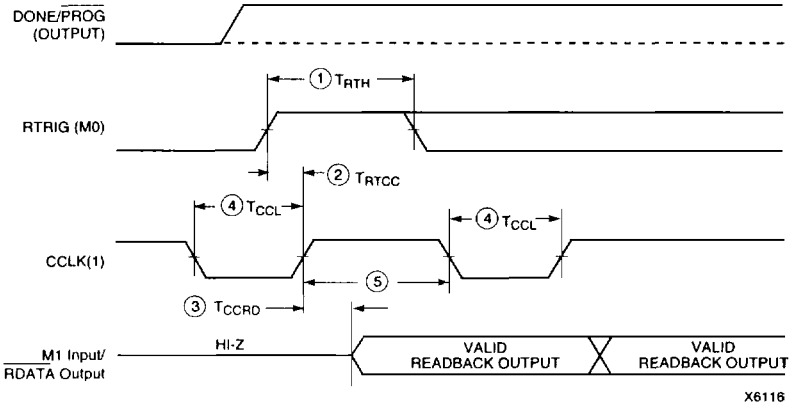
Slave Serial Mode Programming Switching Characteristics



	Description	Symbol		Min	Max	Units
CCLK	To DOUT	3	T_{CCO}		100	ns
	DIN setup	1	T_{DCC}	60		ns
	DIN hold	2	T_{CCD}	0		ns
	High time	4	T_{CCH}	0.05		µs
	Low time (Note 1)	5	T_{CCL}	0.05	5.0	µs
	Frequency		F_{CC}		10	MHz

Notes: 1. The max limit of CCLK Low time is caused by dynamic circuitry inside the LCA device.
2. Configuration must be delayed until the $\overline{INIT}$ of all LCA devices is High.
3. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding $\overline{RESET}$ Low until V_{CC} has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6-µs High level on $\overline{RESET}$, followed by a >6-µs Low level on $\overline{RESET}$ and D/$\overline{P}$ after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).

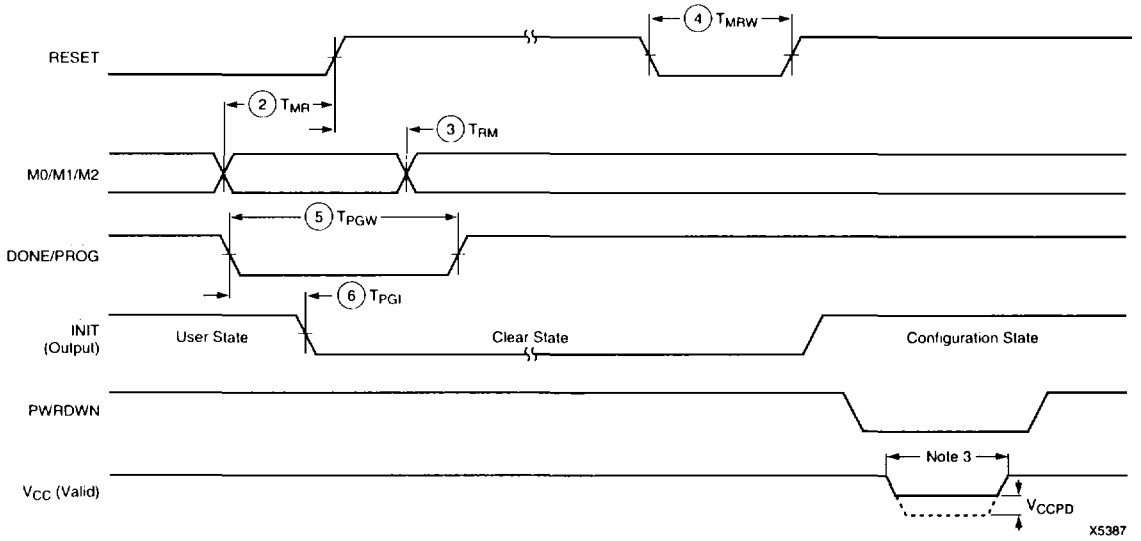
Program Readback Switching Characteristics



	Description	Symbol		Min	Max	Units
RTRIG	RTRIG High	1	T_{RTH}	250		ns
CCLK	RTRIG setup	2	T_{RTCC}	200		ns
	RDATA delay	3	T_{CCRD}		100	ns
	High time	5	T_{CCHR}	0.5		µs
	Low time	4	T_{CCLR}	0.5	5	µs

Notes: 1. During Readback, CCLK frequency may not exceed 1 MHz.
2. RETRIG (M0 positive transition) shall not be done until after one clock following active I/O pins.
3. Readback should not be initiated until configuration is complete.
4. T_{CCLR} is 5 µs min to 15 µs max for XC3000L.

General LCA Switching Characteristics



Description		Symbol		Min	Max	Units
RESET (2)	M0, M1, M2 setup time required	2	T_{MR}	1		µs
	M0, M1, M2 hold time required	3	T_{RM}	3		µs
	RESET Width (Low) req. for Abort	4	T_{MRW}	6		µs
DONE/PROG	Width (Low) required for Re-config.	5	T_{PGW}	6		µs
	INIT response after D/P is pulled Low	6	T_{PGI}		7	µs
PWRDWN (3)	Power Down V_{CC}		V_{CCPD}	2.3		V

Notes: 1. At power-up, V_{cc} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until V_{cc} has reached 4.0 V (2.5 V for XC3000L). A very long V_{cc} rise time of >100 ms, or a non-monotonically rising V_{cc} may require a >1-µs High level on RESET, followed by a >6-µs Low level on RESET and D/P after V_{cc} has reached 4.0 V (2.5 V for XC3000L).

2. RESET timing relative to valid mode lines (M0, M1, M2) is relevant when RESET is used to delay configuration. The specified hold time is caused by a shift-register filter slowing down the response to RESET during configuration.

3. PWRDWN transitions must occur while V_{cc} >4.0 V(2.5 V for XC3000L).

Performance

Device Performance

The XC3000 families of FPGAs can achieve very high performance. This is the result of

- A sub-micron manufacturing process, developed and continuously being enhanced for the production of state-of-the-art CMOS SRAMs.
- Careful optimization of transistor geometries, circuit design, and lay-out, based on years of experience with the XC3000 family.
- A look-up table based, coarse-grained architecture that can collapse multiple-layer combinatorial logic into a single function generator. One CLB can implement up to four layers of conventional logic in as little as 2.7 ns.

Actual system performance is determined by the timing of critical paths, including the delay through the combinatorial and sequential logic elements within CLBs and IOBs, plus the delay in the interconnect routing. The ac-timing specifications state the worst-case timing parameters for the various logic resources available in the XC3000-families architecture. Figure 25 shows a variety of elements involved in determining system performance.

Logic block performance is expressed as the propagation time from the interconnect point at the input to the block to the output of the block in the interconnect area. Since combinatorial logic is implemented with a memory lookup table within a CLB, the combinatorial delay through the CLB, called T_{ILO}, is always the same, regardless of the function being implemented. For the combinatorial logic function driving the data input of the storage element, the critical timing is data set-up relative to the clock edge provided to the flip-flop element. The delay from the clock source to the output of the logic block is critical in the timing signals produced by storage elements. Loading of a logic-block output is limited only by the resulting propagation delay of the larger interconnect network. Speed performance of the logic block is a function of supply voltage and temperature. See Figure 26.

Interconnect performance depends on the routing resources used to implement the signal path. Direct interconnects to the neighboring CLB provide an extremely fast path. Local interconnects go through switch matrices (magic boxes) and suffer an RC delay, equal to the resistance of the pass transistor multiplied by the capacitance of the driven metal line. Longlines carry the signal across the length or breadth of the chip with only one access delay. Generous on-chip signal buffering makes performance relatively insensitive to signal fan-out; increasing fan-out from 1 to 8 changes the CLB delay by only 10%. Clocks can be distributed with two low-skew clock distribution networks.

The tools in the XACT Development System used to place and route a design in an XC3000 FPGA (the Automatic Place and Route [APR] program and the XACT Design Editor)automatically calculate the actual maximum worst-case delays along each signal path. This timing information can be back-annotated to the design's netlist for use in timing simulation or examined with X-DELAY, a static timing analyzer.

Actual system performance is applications dependent. The maximum clock rate that can be used in a system is determined by the critical path delays within that system. These delays are combinations of incremental logic and routing delays, and vary from design to design. In a synchronous system, the maximum clock rate depends on the number of combinatorial logic layers between resynchronizing flip-flops. Figure 27 shows the achievable clock rate as a function of the number of CLB layers.

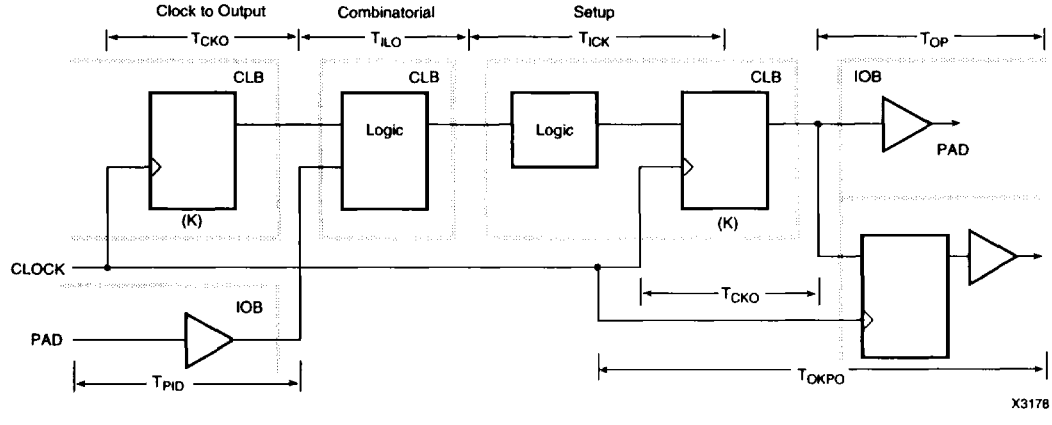


Figure 25. Primary Block Speed Factors. Actual timing is a function of various block factors combined with routing factors. Overall performance can be evaluated with the XACT timing calculator or by an optional simulation.

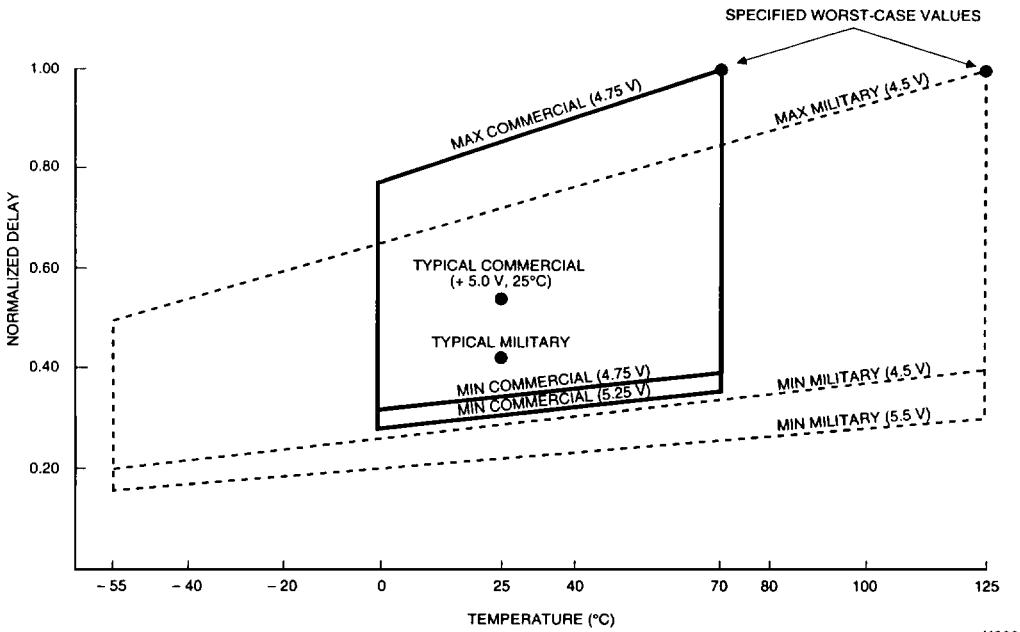


Figure 26. Relative Delay as a Function of Temperature, Supply Voltage and Processing Variations

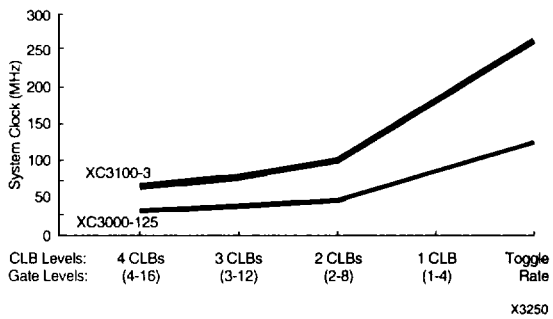


Figure 27. Clock Rate as a Function of Logic Complexity (Number of Combinational Levels between Flip-Flops)

Power

Power Distribution

Power for the LCA device is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the LCA device, a dedicated V_{CC} and ground ring surrounding the logic array provides power to the I/O drivers. An independent matrix of V_{CC} and groundlines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1-µF capacitor connected near the V_{CC} and ground pins will provide adequate decoupling.

Output buffers capable of driving the specified 4- or 8-mA loads under worst-case conditions may be capable of driving as much as 25 to 30 times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The I/O Block output buffers have a slew-limited mode which should be used where output rise and fall times are not speed critical. Slew-limited outputs maintain their dc drive capability, but generate less external reflections and internal noise.

Dynamic Power Consumption

	XC3042	XC3042A	XC3042L	XC3142A	
One CLB driving three local interconnects	0.25	0.17	0.07	0.25	mW per MHz
One global clock buffer and clock line	2.25	1.40	0.50	1.70	mW per MHz
One device output with a 50 pF load	1.25	1.25	0.55	1.25	mW per MHz

Power Consumption

The Logic Cell Array exhibits the low power consumption characteristic of CMOS ICs. For any design, the configuration option of TTL chip input threshold requires power for the threshold reference. The power required by the static memory cells that hold the configuration data is very low and may be maintained in a power-down mode.

Typically, most of power dissipation is produced by external capacitive loads on the output buffers. This load and frequency dependent power is 25 µW/pF/MHz per output. Another component of I/O power is the external dc loading on all output pins.

Internal power dissipation is a function of the number and size of the nodes, and the frequency at which they change. In an LCA device, the fraction of nodes changing on a given clock is typically low (10-20%). For example, in a long binary counter, the total activity of all counter flip-flops is equivalent to that of only two CLB outputs toggling at the clock frequency. Typical global clock-buffer power is between 2.0 mW/MHz for the XC3020 and 3.5 mW/MHz for the XC3090. The internal capacitive load is more a function of interconnect than fan-out. With a typical load of three general interconnect segments, each CLB output requires about 0.25 mW per MHz of its output frequency.

Because the control storage of the Logic Cell Array is CMOS static memory, its cells require a very low standby current for data retention. In some systems, this low data retention current characteristic can be used as a method of preserving configurations in the event of a primary power loss. The Logic Cell Array has built in Powerdown logic which, when activated, will disable normal operation of the device and retain only the configuration data. All internal operation is suspended and output buffers are placed in their high-impedance state with no pull-ups. Different from the XC3000 family which can be powered down to a current consumption of a few microamps, the XC3100 draws 5 mA, even in power-down. This makes power-down operation less meaningful. In contrast, I_{CCPD} for the XC3000L is only 10 µA.

To force the Logic Cell Array into the Powerdown state, the user must pull the $\overline{\text{PWRDWN}}$ pin Low and continue to supply a retention voltage to the V_{CC} pins. When normal power is restored, V_{CC} is elevated to its normal operating voltage and $\overline{\text{PWRDWN}}$ is returned to a High. The Logic Cell Array resumes operation with the same internal sequence that occurs at the conclusion of configuration. Internal-I/O and logic-block storage elements will be reset, the outputs will become enabled and the DONE/$\overline{\text{PROG}}$ pin will be released.

When V_{CC} is shut down or disconnected, some power might unintentionally be supplied from an incoming signal driving an I/O pin. The conventional electrostatic input protection is implemented with diodes to the supply and ground. A positive voltage applied to an input (or output) will cause the positive protection diode to conduct and drive the V_{CC} connection. This condition can produce invalid power conditions and should be avoided. A large series resistor might be used to limit the current or a bipolar buffer may be used to isolate the input signal.

Pin Descriptions

Permanently Dedicated Pins.

V_{CC}
Two to eight (depending on package type) connections to the positive V supply voltage. All must be connected.

GND
Two to eight (depending on package type) connections to ground. All must be connected.

PWRDWN
A Low on this CMOS-compatible input stops all internal activity, but retains configuration. All flip-flops and latches are reset, all outputs are 3-stated, and all inputs are interpreted as High, independent of their actual level. When PWDWN returns High, the LCA device becomes operational with DONE Low for two cycles of the internal 1-MHz clock.Before and during configuration, PWRDWN must be High. If not used, PWRDWN must be tied to V_{CC}.

RESET
This is an active Low input which has three functions.

Prior to the start of configuration, a Low input will delay the start of the configuration process. An internal circuit senses the application of power and begins a minimal time-out cycle. When the time-out and RESET are complete, the levels of the M lines are sampled and configuration begins.

If RESET is asserted during a configuration, the LCA device is re-initialized and restarts the configuration at the termination of RESET.

If RESET is asserted after configuration is complete, it provides a global asynchronous RESET of all IOB and CLB storage elements of the LCA device.

CCLK
During configuration, Configuration Clock is an output of an LCA device in Master mode or Peripheral mode, but an input in Slave mode. During Readback, CCLK is a clock input for shifting configuration data out of the LCA device

CCLK drives dynamic circuitry inside the LCA device. The Low time may, therefore, not exceed a few microseconds. When used as an input, CCLK must be "parked High". An internal pull-up resistor maintains High when the pin is not being driven.

DONE/PROG (D/P)
DONE is an open-drain output, configurable with or without an internal pull-up resistor of 2 to 8 k Ω. At the completion of configuration, the LCA device circuitry becomes active in a synchronous order; DONE is programmed to go active High one cycle either before or after the outputs go active.

Once configuration is done, a High-to-Low transition of this pin will cause an initialization of the LCA device and start a reconfiguration.

M0/RTRIG
As Mode 0, this input is sampled on power-on to determine the power-on delay (2^{14} cycles if M0 is High, 2^{16} cycles if M0 is Low). Before the start of configuration, this input is again sampled together with M1, M2 to determine the configuration mode to be used .

A Low-to-High input transition, after configuration is complete, acts as a Read Trigger and initiates a Readback of configuration and storage-element data clocked by CCLK. By selecting the appropriate Readback option when generating the bitstream, this operation may be limited to a single Readback, or be inhibited altogether.

M1/RDATA
As Mode 1, this input and M0, M2 are sampled before the start of configuration to establish the configuration mode to be used. If Readback is never used, M1 can be tied directly to ground or V_{CC}. If Readback is ever used, M1 must use a 5-kΩ resistor to ground or V_{CC}, to accommodate the RDATA output.

As an active-Low Read Data, after configuration is complete, this pin is the output of the Readback data.

User I/O Pins that can have special functions.

M2
During configuration, this input has a weak pull-up resistor. Together with M0 and M1, it is sampled before the start of configuration to establish the configuration mode to be used. After configuration, this pin is a user-programmable I/O pin.

HDC
During configuration, this output is held at a High level to indicate that configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin.

$\overline{LDC}$
During Configuration, this output is held at a Low level to indicate that the configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin. $\overline{LDC}$ is particularly useful in Master mode as a Low enable for an EPROM, but it must then be programmed as a High after configuration.

$\overline{INIT}$
This is an active Low open-drain output with a weak pull-up and is held Low during the power stabilization and internal clearing of the configuration memory. It can be used to indicate status to a configuring microprocessor or, as a wired AND of several slave mode devices, a hold-off signal for a master mode device. After configuration this pin becomes a user-programmable I/O pin.

BCLKIN
This is a direct CMOS level input to the alternate clock buffer (Auxiliary Buffer) in the lower right corner.

XTL1
This user I/O pin can be used to operate as the output of an amplifier driving an external crystal and bias circuitry.

XTL2
This user I/O pin can be used as the input of an amplifier connected to an external crystal and bias circuitry. The I/O Block is left unconfigured. The oscillator configuration is activated by routing a net from the oscillator buffer symbol output and by the MakeBits program.

$\overline{CS0}$, $\overline{CS1}$, CS2, $\overline{WS}$
These four inputs represent a set of signals, three active Low and one active High, that are used to control configuration-data entry in the Peripheral mode. Simultaneous assertion of all four inputs generates a Write to the internal data buffer. The removal of any assertion clocks in the D0-D7 data. In Master-Parallel mode, WS and CS2 are the A0 and A1 outputs. After configuration, these pins are user-programmable I/O pins.

RDY/$\overline{BUSY}$
During Peripheral Parallel mode configuration this pin indicates when the chip is ready for another byte of data to be written to it. After configuration is complete, this pin becomes a user-programmed I/O pin.

$\overline{RCLK}$
During Master Parallel mode configuration, each change on the A0-15 outputs is preceded by a rising edge on $\overline{RCLK}$, a redundant output signal. After configuration is complete, this pin becomes a user-programmed I/O pin.

D0-D7
This set of eight pins represents the parallel configuration byte for the parallel Master and Peripheral modes. After configuration is complete, they are user-programmed I/O pins.

A0-A15
During Master Parallel mode, these 16 pins present an address output for a configuration EPROM. After configuration, they are user-programmable I/O pins.

DIN
During Slave or Master Serial configuration, this pin is used as a serial-data input. In the Master or Peripheral configuration, this is the Data 0 input. After configuration is complete, this pin becomes a user-programmed I/O pin.

DOUT
During configuration this pin is used to output serial-configuration data to the DIN pin of a daisy-chained slave. After configuration is complete, this pin becomes a user-programmed I/O pin.

TCLKIN
This is a direct CMOS-level input to the global clock buffer. This pin can also be configured as a user programmable I/O pin. However, since TCLKIN is the preferred input to the global clock net, and the global clock net should be used as the primary clock source, this pin is usually the clock input to the chip.

Unrestricted User I/O Pins.

I/O
An I/O pin may be programmed by the user to be an Input or an Output pin following configuration. All unrestricted I/O pins, plus the special pins mentioned on the following page, have a weak pull-up resistor of 50 kΩ to 100 kΩ that becomes active as soon as the device powers up, and stays active until the end of configuration.

Before and during configuration, all outputs that are not used for the configuration process are 3-stated with a 50 kΩ to 100 kΩ pull-up resistor.

Pin Functions During Configuration

Configuration Mode <M2:M1:M0>					***									****	
SLAVE <1:1:1>	MASTER-SER <0:0:0>	PERIPHERAL <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>	44 PLCC	68 PLCC	84 PLCC	84 PGA	100 PQFP	100 TQFP	132 PGA	160 PQFP	175 PGA	208 PQFP	User Operation
PWRDWN (I)	PWRDWN (I)	PWRDWN (I)	PWRDWN (I)	PWRDWN (I)	7	10	12	B2	29	26	A1	159	B2	3	PWRDWN (I)
VCC	VCC	VCC	VCC	VCC	12	18	22	F3	41	38	C8	20	D9	26	VCC
M1 (HIGH) (I)	M1 (LOW) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	16	25	31	J2	52	49	B13	40	B14	48	RDATA
M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	M0 (LOW) (I)	17	26	32	L1	54	51	A14	42	B15	50	RTRIG (I)
M2 (HIGH) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	18	27	33	K2	56	53	C13	44	C15	56	I/O
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	19	28	34	K3	57	54	B14	45	E14	57	I/O
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	20	30	36	L3	59	56	D14	49	D16	61	I/O
INIT*	INIT*	INIT*	INIT*	INIT*	22	34	42	K6	65	62	G14	59	H15	77	I/O
GND	GND	GND	GND	GND	23	35	43	J6	66	63	H12	19	J14	79	GND
					26	43	53	L11	76	73	M13	76	P15	100	XTL2 OR I/O
RESET (I)	RESET (I)	RESET (I)	RESET (I)	RESET (I)	27	44	54	K10	78	75	P14	78	R15	102	RESET (I)
DONE	DONE	DONE	DONE	DONE	28	45	55	J10	80	77	N13	80	R14	107	PROGRAM (I)
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)		46	56	K11	81	78	M12	81	N13	109	I/O
					30	47	57	J11	82	79	P13	82	T14	110	XTL1 OR I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)		48	58	H10	83	80	N11	86	P12	115	I/O
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)		49	60	F10	87	84	M9	92	T11	122	I/O
		CS0 (I)				50	61	G10	88	85	N9	93	R10	123	I/O
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)		51	62	G11	89	86	N8	98	R9	128	I/O
VCC	VCC	VCC	VCC	VCC	34	52	64	F9	91	88	M8	100	N9	130	Vcc
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)		53	65	F11	92	89	N7	102	P8	132	I/O
		CS1 (I)				54	66	E11	93	90	P6	103	R8	133	I/O
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)		55	67	E10	94	91	M6	108	R7	138	I/O
		DATA 1 (I)	DATA 1 (I)	DATA 1 (I)		56	70	D10	98	95	M5	114	R5	145	I/O
		RDY/BUSY	RCLK	RCLK		57	71	C11	99	96	N4	115	P5	146	I/O
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	38	58	72	B11	100	97	N2	119	R3	151	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	39	59	73	C10	1	98	M3	120	N4	152	I/O
CCLK (I)	CCLK(O)	CCLK(O)	CCLK(O)	CCLK(O)	40	60	74	A11	2	99	P1	121	R2	153	CCLK (I)
		WS (I)	A0	A0		61	75	B10	5	2	M2	124	P2	161	I/O
		CS2 (I)	A1	A1		62	76	B9	6	3	N1	125	M3	162	I/O
			A2	A2		63	77	A10	8	5	L2	128	P1	165	I/O
			A3	A3		64	78	A9	9	6	L1	129	N1	166	I/O
			A15	A15		65	81	B8	12	9	K1	132	M1	172	I/O
			A4	A4		66	82	B7	13	10	J2	133	L2	173	I/O
			A14	A14		67	83	A7	14	11	H1	136	K2	178	I/O
			A5	A5		68	84	C7	15	12	H2	137	K1	179	I/O
GND	GND	GND	GND	GND	1	1	1	C6	16	13	H3	139	J3	182	GND
			A13	A13		2	2	A6	17	14	G2	141	H2	184	I/O
			A6	A6		3	3	A5	18	15	G1	142	H1	185	I/O
			A12	A12		4	4	B5	19	16	F2	147	F2	192	I/O
			A7	A7		5	5	C5	20	17	E1	148	E1	193	I/O
			A11	A11		6	8	A3	23	20	D1	151	D1	199	I/O
			A8	A8		7	9	A2	24	21	D2	152	C1	200	I/O
			A10	A10		8	10	B3	25	22	B1	155	E3	203	I/O
			A9	A9		9	11	A1	26	26	C2	156	C2	204	I/O
															All Others
						X	X	X	X						XC3020 etc.
					X	X	X	X	X	X					XC3030 etc.
							X	X	X	X	X				XC3042 etc.
							X**				X				XC3064 etc.
							X**					X	X	X	XC3090 etc.
							X**					X	X	X	XC3195

X5268

Represents a 50-kΩ to 100-kΩ pull-up before and during configuration

* INIT is an open drain output during configuration

(I) Represents an input

** Pin assignmnent for the XC3064/XC3090 and XC3195 differ from those shown. See page 2-138.

*** Peripheral mode and master parallel mode are not supported in the PC44 package. See page 2-135.

**** Pin assignments for the XC3195 PQ208 differ from those shown. See page 2-146.

Pin assignments of PGA Footprint PLCC sockets and PGA packages are not electrically identical.

Generic I/O pins are not shown.

The information on this page is provided as a convenient summary. For detailed pin descriptions, see the preceding two pages.

For a detailed description of the configuration modes, see pages 2-190 through 2-200.

For pinout details, see pages 2-136 through 2-146.

Before and during configuration, all outputs that are not used for the configuration process are 3-stated with a 50 kΩ to 100 kΩ pull-up resistor.

XC3000 Families Pin Assignments

Xilinx offers the six different array sizes in the XC3000 families in a variety of surface-mount and through-hole package types, with pin counts from 44 to 223.

Each chip is offered in several package types to accommodate the available PC board space and manufacturing technology. Most package types are also offered with different chips to accommodate design changes without the need for PC board changes.

Note that there is no perfect match between the number of bonding pads on the chip and the number of pins on a package. In some cases, the chip has more pads than there are pins on the package, as indicated by the information ("unused" pads) below the line in the following table. The IOBs of the unconnected pads can still be used as storage elements if the specified propagation delays and set-up times are acceptable.

In other cases, the chip has fewer pads than there are pins on the package; therefore, some package pins are not connected (n.c.), as shown above the line in the following table.

Number of Unbounded or Unconnected Pins

		Number of Package Pins											
Device	**Pads**	**44**	**64**	**68**	**84**	**100**	**132**	**144**	**160**	**175**	**176**	**208**	**223**
3020	74	—	—	6 u	10 n.c.	26 n.c.	—	—	—	—	—	—	—
3030	98	54 u	34 u	30 u	14 u	2 n.c.	—	—	—	—	—	—	—
3042	118	—	—	—	34 u	18 u	14 n.c.	26 n.c.	—	—	—	—	—
3064	142	—	—	—	50 u	—	10 u	2 u	18 n.c.	—	—	—	—
3090	166	—	—	—	82 u	—	—	—	6 u	9 n.c	10 n.c.	42 n.c.	—
3195	198	—	—	—	114 u	—	—	—	—	9 n.c. 32 u	—	10 n.c.	25 n.c.

n.c. = Unconnected package pin
u = Unbonded device pad

X6095

Number of Available I/O Pins

		Number of Package Pins																
	Max I/O	**44**	**64**	**68**	**84**	**100**	**120**	**132**	**144**	**156**	**160**	**164**	**175**	**176**	**191**	**196**	**208**	**223**	**240**
XC3020/XC3120	64			58	64	64													
XC3030/XC3130	80	34	54	58	74	80													
XC3042/XC3142	96				74	82		96											
XC3064/XC3164	120				70			110			120								
XC3090/XC3190	144				70						138	142	144	144			144		
XC3195	176				70						138		144				176	176	

X3478

XC3000 Family 44-Pin PLCC Pinouts

XC3000, XC3000A, XC3000L, XC3100 and XC3100A families have identical pinouts

Pin No.	XC3030
1	**GND**
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	$\overline{\text{PWRDWN}}$
8	TCLKIN-I/O
9	I/O
10	I/O
11	I/O
12	**VCC**
13	I/O
14	I/O
15	I/O
16	M1-$\overline{\text{RDATA}}$
17	M0-RTRIG
18	M2-I/O
19	HDC-I/O
20	$\overline{\text{LDC}}$-I/O
21	I/O
22	$\overline{\text{INIT}}$-I/O

Pin No.	XC3030
23	**GND**
24	I/O
25	I/O
26	XTL2(IN)-I/O
27	$\overline{\text{RESET}}$
28	DONE-$\overline{\text{PGM}}$
29	I/O
30	XTL1(OUT)-BCLK-I/O
31	I/O
32	I/O
33	I/O
34	**VCC**
35	I/O
36	I/O
37	I/O
38	DIN-I/O
39	DOUT-I/O
40	CCLK
41	I/O
42	I/O
43	I/O
44	I/O

Peripheral mode and Master Parallel mode are not supported in the PC44 package

XC3030 Family 64-Pin Plastic VQFP Pinouts

XC3000, XC3000A, XC3000L and XC3100 families have identical pinouts

Pin No.	XC3030
1	A0-$\overline{\text{WS}}$-I/O
2	A1-$\overline{\text{CS2}}$-I/O
3	A2-I/O
4	A3-I/O
5	A4-I/O
6	A14-I/O
7	A5-I/O
8	**GND**
9	A13-I/O
10	A6-I/O
11	A12-I/O
12	A7-I/O
13	A11-I/O
14	A8-I/O
15	A10-I/O
16	A9-I/O
17	$\overline{\text{PWRDN}}$
18	TCLKIN-I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	**VCC**
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1-$\overline{\text{RDATA}}$
32	M0-RTRIG

Pin No.	XC3030
33	M2-I/O
34	HDC-I/O
35	I/O
36	$\overline{\text{LDC}}$-I/O
37	I/O
38	I/O
39	I/O
40	$\overline{\text{INIT}}$-I/O
41	**GND**
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	XTAL2(IN)-I/O
48	$\overline{\text{RESET}}$
49	DONE-$\overline{\text{PG}}$
50	D7-I/O
51	XTAL1(OUT)-BCLKIN-I/O
52	D6-I/O
53	D5-I/O
54	$\overline{\text{CS0}}$-I/O
55	D4-I/O
56	**VCC**
57	D3-I/O
58	$\overline{\text{CS1}}$-I/O
59	D2-I/O
60	D1-I/O
61	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O
62	D0-DIN-I/O
63	DOUT-I/O
64	CCLK

XC3000 Families 68-Pin PLCC, 84-Pin PLCC and PGA Pinouts

XC3000, XC3000A, XC3000L, XC3100 and XC3100A families have identical pinouts

68 PLCC XC3030	68 PLCC XC3020	XC3020 XC3030, XC3042	84 PLCC	84 PGA
10	10	PWRDN	12	B2
11	11	TCLKIN-I/O	13	C2
12	—	**I/O***	14	B1
13	12	I/O	15	C1
14	13	I/O	16	D2
—	—	I/O	17	D1
15	14	I/O	18	E3
16	15	I/O	19	E2
—	16	I/O	20	E1
17	17	I/O	21	F2
18	18	**VCC**	22	F3
19	19	I/O	23	G3
—	—	I/O	24	G1
20	20	I/O	25	G2
—	21	I/O	26	F1
21	22	I/O	27	H1
22	—	I/O	28	H2
23	23	I/O	29	J1
24	24	I/O	30	K1
25	25	M1-RDATA	31	J2
26	26	M0-RTRIG	32	L1
27	27	M2-I/O	33	K2
28	28	HDC-I/O	34	K3
29	29	I/O	35	L2
30	30	LDC-I/O	36	L3
—	31	I/O	37	K4
—		**I/O***	38	L4
31	32	I/O	39	J5
32	33	I/O	40	K5
33	—	**I/O***	41	L5
34	34	INIT-I/O	42	K6
35	35	**GND**	43	J6
36	36	I/O	44	J7
37	37	I/O	45	L7
38	38	I/O	46	K7
39	39	I/O	47	L6
—	40	I/O	48	L8
—	41	I/O	49	K8
40		**I/O***	50	L9
41		**I/O***	51	L10
42	42	I/O	52	K9
43	43	XTL2(IN)-I/O	53	L11

68 PLCC XC3030 XC3020	XC3020 XC3030, XC3042	84 PLCC	84 PGA
44	RESET	54	K10
45	DONE-PG	55	J10
46	D7-I/O	56	K11
47	XTL1(OUT)-BCLKIN-I/O	57	J11
48	D6-I/O	58	H10
—	I/O	59	H11
49	D5-I/O	60	F10
50	CS0-I/O	61	G10
51	D4-I/O	62	G11
—	I/O	63	G9
52	**VCC**	64	F9
53	D3-I/O	65	F11
54	CS1-I/O	66	E11
55	D2-I/O	67	E10
—	I/O	68	E9
—	**I/O***	69	D11
56	D1-I/O	70	D10
57	RDY/BUSY-RCLK-I/O	71	C11
58	D0-DIN-I/O	72	B11
59	DOUT-I/O	73	C10
60	CCLK	74	A11
61	A0-WS-I/O	75	B10
62	A1-CS2-I/O	76	B9
63	A2-I/O	77	A10
64	A3-I/O	78	A9
—	**I/O***	79	B8
—	**I/O***	80	A8
65	A15-I/O	81	B6
66	A4-I/O	82	B7
67	A14-I/O	83	A7
68	A5-I/O	84	C7
1	**GND**	1	C6
2	A13-I/O	2	A6
3	A6-I/O	3	A5
4	A12-I/O	4	B5
5	A7-I/O	5	C5
—	**I/O***	6	A4
—	**I/O***	7	B4
6	A11-I/O	8	A3
7	A8-I/O	9	A2
8	A10-I/O	10	B3
9	A9-I/O	11	A1

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

This table describes the pinouts of three different chips in three different packages. The pin-description column lists 84 of the 118 pads on the XC3042 (and 84 of the 98 pads on the XC3030) that are connected to the 84 package pins. Ten pads, indicated by an asterisk, do not exist on the XC3020, which has 74 pads; therefore the corresponding pins on the 84-pin packages have no connections to an XC3020. Six pads on the XC3020 and 16 pads on the XC3030, indicated by a dash (—) in the 68 PLCC column, have no connection to the 68 PLCC, but are connected to the 84-pin packages.

XC3064/XC3090/XC3195 84-Pin PLCC Pinouts

XC3000, XC3000A, XC3000L, XC3100 and XC3100A families have identical pinouts

PLCC Pin Number	XC3064, XC3090, XC3195
12	$\overline{PWRDN}$
13	TCLKIN-I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	**GND***
22	VCC
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1-$\overline{RDATA}$
32	M0-RTRIG
33	M2-I/O
34	HDC-I/O
35	I/O
36	$\overline{LDC}$-I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	INIT/I/O*
42	**VCC***
43	**GND**
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	I/O
53	XTL2(IN)-I/O

PLCC Pin Number	XC3064, XC3090, XC3195
54	$\overline{RESET}$
55	DONE-$\overline{PG}$
56	D7-I/O
57	XTL1(OUT)-BCLKIN-I/O
58	D6-I/O
59	I/O
60	D5-I/O
61	$\overline{CS0}$-I/O
62	D4-I/O
63	I/O
64	VCC
65	**GND***
66	D3-I/O*
67	$\overline{CS1}$-I/O*
68	D2-I/O*
69	I/O
70	D1-I/O
71	RDY/$\overline{BUSY}$-$\overline{RCLK}$-I/O
72	D0-DIN-I/O
73	DOUT-I/O
74	CCLK
75	A0-$\overline{WS}$-I/O
76	A1-CS2-I/O
77	A2-I/O
78	A3-I/O
79	I/O
80	I/O
81	A15-I/O
82	A4-I/O
83	A14-I/O
84	A5-I/O
1	**GND**
2	**VCC***
3	A13-I/O*
4	A6-I/O*
5	A12-I/O*
6	A7-I/O*
7	I/O
8	A11-I/O
9	A8-I/O
10	A10-I/O
11	A9-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed ouptuts are default slew-rate limited.

* In the PC84 package, XC3064, XC3090 and XC3195 have additional V_{CC} and GND pins and thus a different pin definition than XC3020/XC3030/XC3042.

XC3000 Families 100-Pin QFP Pinouts

XC3000, XC3000A, XC3000L, XC3100 and XC3100A families have identical pinouts

Pin No.			XC3020 XC3030 XC3042
CQFP	PQFP	TQFP VQFP	
1	16	13	GND
2	17	14	A13-I/O
3	18	15	A6-I/O
4	19	16	A12-I/O
5	20	17	A7-I/O
6	21	18	I/O*
7	22	19	I/O*
8	23	20	A11-I/O
9	24	21	A8-I/O
10	25	22	A10-I/O
11	26	23	A9-I/O
12	27	24	VCC*
13	28	25	GND*
14	29	26	PWRDN
15	30	27	TCLKIN-I/O
16	31	28	I/O**
17	32	29	I/O*
18	33	30	I/O*
19	34	31	I/O
20	35	32	I/O
21	36	33	I/O
22	37	34	I/O
23	38	35	I/O
24	39	36	I/O
25	40	37	I/O
26	41	38	VCC
27	42	39	I/O
28	43	40	I/O
29	44	41	I/O
30	45	42	I/O
31	46	43	I/O
32	47	44	I/O
33	48	45	I/O
34	49	46	I/O

Pin No.			XC3020 XC3030 XC3042
CQFP	PQFP	TQFP VQFP	
35	50	47	I/O*
36	51	48	I/O*
37	52	49	M1-RD
38	53	50	GND*
39	54	51	MO-RT
40	55	52	VCC*
41	56	53	M2-I/O
42	57	54	HDC-I/O
43	58	55	I/O
44	59	56	LDC-I/O
45	60	57	I/O*
46	61	58	I/O*
47	62	59	I/O
48	63	60	I/O
49	64	61	I/O
50	65	62	INIT-I/O
51	66	63	GND
52	67	64	I/O
53	68	65	I/O
54	69	66	I/O
55	70	67	I/O
56	71	68	I/O
57	72	69	I/O
58	73	70	I/O
59	74	71	I/O*
60	75	72	I/O*
61	76	73	XTL2-I/O
62	77	74	GND*
63	78	75	RESET
64	79	76	VCC*
65	80	77	DONE-PG
66	81	78	D7-I/O
67	82	79	BCLKIN-XTL1-I/O
68	83	80	D6-I/O

Pin No.			XC3020 XC3030 XC3042
CQFP	PQFP	TQFP VQFP	
69	84	81	I/O*
70	85	82	I/O*
71	86	83	I/O
72	87	84	D5-I/O
73	88	85	CS0-I/O
74	89	86	D4-I/O
75	90	87	I/O
76	91	88	VCC
77	92	89	D3-I/O
78	93	90	CS1-I/O
79	94	91	D2-I/O
80	95	92	I/O
81	96	93	I/O*
82	97	94	I/O*
83	98	95	D1-I/O
84	99	96	RDY/BUSY-RCLK-I/O
85	100	97	DO-DIN-I/O
86	1	98	DOUT-I/O
87	2	99	CCLK
88	3	100	VCC*
89	4	1	GND*
90	5	2	AO-WS-I/O
91	6	3	A1-CS2-I/O
92	7	4	I/O**
93	8	5	A2-I/O
94	9	6	A3-I/O
95	10	7	I/O*
96	11	8	I/O*
97	12	9	A15-I/O
98	13	10	A4-I/O
99	14	11	A14-I/O
100	15	12	A5-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* This table describes the pinouts of three different chips in three different packges. The pin-description column lists 100 of the 118 pads on the XC3042 that are connected to the 100 package pins. Two pads, indicated by double asterisks, do not exist on the XC3030, which has 98 pads; therefore the corresponding pins have no connections. Twenty-six pads, indicated by single or double asterisks, do not exist on the XC3020, which has 74 pads; therefore, the corresponding pins have no connections. (See table on page 2-139.)

XC3000 Families 132-Pin Ceramic and Plastic PGA Pinouts

XC3000, XC3000A, XC3000L, XC3100 and XC3100A families have identical pinouts

PGA Pin Number	XC3042 XC3064	PGA Pin Number	XC3042 XC3064	PGA Pin Number	XC3042 XC3064	PGA Pin Number	XC3042 XC3064
C4	**GND**	B13	M1-$\overline{RD}$	P14	$\overline{RESET}$	M3	DOUT-I/O
A1	$\overline{PWRDN}$	C11	**GND**	M11	**VCC**	P1	CCLK
C3	I/O-TCLKIN	A14	M0-RT	N13	DONE-$\overline{PG}$	M4	**VCC**
B2	I/O	D12	**VCC**	M12	D7-I/O	L3	**GND**
B3	I/O	C13	M2-I/O	P13	XTL1-I/O-BCLKIN	M2	A0-$\overline{WS}$-I/O
A2	**I/O***	B14	HDC-I/O	N12	I/O	N1	A1-CS2-I/O
B4	I/O	C14	I/O	P12	I/O	M1	I/O
C5	I/O	E12	I/O	N11	D6-I/O	K3	I/O
A3	**I/O***	D13	I/O	M10	I/O	L2	A2-I/O
A4	I/O	D14	$\overline{LDC}$-I/O	P11	**I/O***	L1	A3-I/O
B5	I/O	E13	**I/O***	N10	I/O	K2	I/O
C6	I/O	F12	I/O	P10	I/O	J3	I/O
A5	I/O	E14	I/O	M9	D5-I/O	K1	A15-I/O
B6	I/O	F13	I/O	N9	$\overline{CS0}$-I/O	J2	A4-I/O
A6	I/O	F14	I/O	P9	**I/O***	J1	**I/O***
B7	I/O	G13	I/O	P8	**I/O***	H1	A14-I/O
C7	**GND**	G14	$\overline{INIT}$-I/O	N8	D4-I/O	H2	A5-I/O
C8	**VCC**	G12	**VCC**	P7	I/O	H3	**GND**
A7	I/O	H12	**GND**	M8	**VCC**	G3	**VCC**
B8	I/O	H14	I/O	M7	**GND**	G2	A13-I/O
A8	I/O	H13	I/O	N7	D3-I/O	G1	A6-I/O
A9	I/O	J14	I/O	P6	$\overline{CS1}$-I/O	F1	**I/O***
B9	I/O	J13	I/O	N6	**I/O***	F2	A12-I/O
C9	I/O	K14	I/O	P5	**I/O***	E1	A7-I/O
A10	I/O	J12	I/O	M6	D2-I/O	F3	I/O
B10	I/O	K13	I/O	N5	I/O	E2	I/O
A11	**I/O***	L14	**I/O***	P4	I/O	D1	A11-I/O
C10	I/O	L13	I/O	P3	I/O	D2	A8-I/O
B11	I/O	K12	I/O	M5	D1-I/O	E3	I/O
A12	**I/O***	M14	I/O	N4	RDY/$\overline{BUSY}$-RCLK-I/O	C1	I/O
B12	I/O	N14	I/O	P2	I/O	B1	A10-I/O
A13	**I/O***	M13	XTL2(IN)-I/O	N3	I/O	C2	A9-I/O
C12	I/O	L12	**GND**	N2	D0-DIN-I/O	D3	**VCC**

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* Indicates unconnected package pins (14) for the XC3042.

XC3000 Families 144-Pin Plastic TQFP Pinouts

XC3000, XC3000A, XC3000L, XC3100 and XC3100A families have identical pinouts

Pin Number	XC3042 XC3064
1	PWRDN
2	I/O-TCLKIN
3	I/O*
4	I/O
5	I/O
6	I/O*
7	I/O
8	I/O
9	I/O*
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O*
16	I/O
17	I/O
18	GND
19	VCC
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O*
29	I/O
30	I/O
31	I/O*
32	I/O*
33	I/O
34	I/O*
35	I/O
36	M1-RD
37	GND
38	MO-RT
39	VCC
40	M2-I/O
41	HDC-I/O
42	I/O
43	I/O
44	I/O
45	LDC-I/O
46	I/O*
47	I/O
48	I/O

Pin Number	XC3042 XC3064
49	I/O
50	I/O*
51	I/O
52	I/O
53	INIT-I/O
54	VCC
55	GND
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O*
64	I/O*
65	I/O
66	I/O
67	I/O
68	I/O
69	XTL2(IN)-I/O
70	GND
71	RESET
72	VCC
73	DONE-PG
74	D7-I/O
75	XTL1(OUT)-BCLKIN-I/O
76	I/O
77	I/O
78	D6-I/O
79	I/O
80	I/O*
81	I/O
82	I/O
83	I/O*
84	D5-I/O
85	CS0-I/O
86	I/O*
87	I/O*
88	D4-I/O
89	I/O
90	VCC
91	GND
92	D3-I/O
93	CS1-I/O
94	I/O*
95	I/O*
96	D2-I/O

Pin Number	XC3042 XC3064
97	I/O
98	I/O
99	I/O*
100	I/O
101	I/O*
102	D1-I/O
103	RDY/BUSY-RCLK-I/O
104	I/O
105	I/O
106	D0-DIN-I/O
107	DOUT-I/O
108	CCLK
109	VCC
110	GND
111	A0-WS I/O
112	A1-CS2-I/O
113	I/O
114	I/O
115	A2-I/O
116	A3-I/O
117	I/O
118	I/O
119	A15-I/O
120	A4-I/O
121	I/O*
122	I/O*
123	A14-I/O
124	A5-I/O
125	-
126	GND
127	VCC
128	A13-I/O
129	A6-I/O
130	I/O*
131	-
132	I/O*
133	A12-I/O
134	A7-I/O
135	I/O
136	I/O
137	A11-I/O
138	A8-I/O
139	I/O
140	I/O
141	A10-I/O
142	A9-I/O
143	VCC
144	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* Indicates unconnected package pins (24) for the XC3042.

XC3000 Families160-Pin PQFP Pinouts

XC3000, XC3000A, XC3000L, XC3100 and XC3100A families have identical pinouts

PQFP Pin Number	XC3064, XC3090, XC3195
1	I/O*
2	I/O*
3	I/O*
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	GND
20	VCC
21	I/O*
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O*
39	I/O*
40	M1-RDATA

PQFP Pin Number	XC3064, XC3090, XC3195
41	GND
42	M0-RTRIG
43	VCC
44	M2-I/O
45	HDC-I/O
46	I/O
47	I/O
48	I/O
49	LDC-I/O
50	I/O*
51	I/O*
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	INIT-I/O
60	VCC
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O*
76	XTL2-I/O
77	GND
78	RESET
79	VCC
80	DONE/PG

PQFP Pin Number	XC3064, XC3090, XC3195
81	D7-I/O
82	XTL1-I/O-BCLKIN
83	I/O*
84	I/O
85	I/O
86	D6-I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	D5-I/O
93	CS0-I/O
94	I/O*
95	I/O*
96	I/O
97	I/O
98	D4-I/O
99	I/O
100	VCC
101	GND
102	D3-I/O
103	CS1-I/O
104	I/O
105	I/O
106	I/O*
107	I/O*
108	D2-I/O
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	D1-I/O
115	RDY/BUSY-RCLK-I/O
116	I/O
117	I/O
118	I/O*
119	D0-DIN-I/O
120	DOUT-I/O

PQFP Pin Number	XC3064, XC3090, XC3195
121	CCLK
122	VCC
123	GND
124	A0-WS-I/O
125	A1-CS2-I/O
126	I/O
127	I/O
128	A2-I/O
129	A3-I/O
130	I/O
131	I/O
132	A15-I/O
133	A4-I/O
134	I/O
135	I/O
136	A14-I/O
137	A5-I/O
138	I/O*
139	GND
140	VCC
141	A13-I/O
142	A6-I/O
143	I/O*
144	I/O*
145	I/O
146	I/O
147	A12-I/O
148	A7-I/O
149	I/O
150	I/O
151	A11-I/O
152	A8-I/O
153	I/O
154	I/O
155	A10-I/O
156	A9-I/O
157	VCC
158	GND
159	PWRDWN
160	TCLKIN-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed IOBs are default slew-rate limited.

*Indicates unconnected package pins (18) for the XC3064.

XC3000 Families 175-Pin Ceramic and Plastic PGA Pinouts

XC3000, XC3000A, XC3000L, XC3100 and XC3100A families have identical pinouts

PGA Pin Number	XC3090, XC3195
B2	PWRDN
D4	TCLKIN-I/O
B3	I/O
C4	I/O
B4	I/O
A4	I/O
D5	I/O
C5	I/O
B5	I/O
A5	I/O
C6	I/O
D6	I/O
B6	I/O
A6	I/O
B7	I/O
C7	I/O
D7	I/O
A7	I/O
A8	I/O
B8	I/O
C8	I/O
D8	GND
D9	VCC
C9	I/O
B9	I/O
A9	I/O
A10	I/O
D10	I/O
C10	I/O
B10	I/O
A11	I/O
B11	I/O
D11	I/O
C11	I/O
A12	I/O
B12	I/O
C12	I/O
D12	I/O
A13	I/O
B13	I/O
C13	I/O
A14	I/O

PGA Pin Number	XC3090, XC3195
D13	I/O
B14	M1-RDATA
C14	GND
B15	M0-RTRIG
D14	VCC
C15	M2-I/O
E14	HDC-I/O
B16	I/O
D15	I/O
C16	I/O
D16	LDC-I/O
F14	I/O
E15	I/O
E16	I/O
F15	I/O
F16	I/O
G14	I/O
G15	I/O
G16	I/O
H16	I/O
H15	INIT-I/O
H14	VCC
J14	GND
J15	I/O
J16	I/O
K16	I/O
K15	I/O
K14	I/O
L16	I/O
L15	I/O
M16	I/O
M15	I/O
L14	I/O
N16	I/O
P16	I/O
N15	I/O
R16	I/O
M14	I/O
P15	XTL2(IN)-I/O
N14	GND
R15	RESET
P14	VCC

PGA Pin Number	XC3090, XC3195
R14	DONE-PG
N13	D7-I/O
T14	XTL1(OUT)-BCLKIN-I/O
P13	I/O
R13	I/O
T13	I/O
N12	I/O
P12	D6-I/O
R12	I/O
T12	I/O
P11	I/O
N11	I/O
R11	I/O
T11	D5-I/O
R10	CS0-I/O
P10	I/O
N10	I/O
T10	I/O
T9	I/O
R9	D4-I/O
P9	I/O
N9	VCC
N8	GND
P8	D3-I/O
R8	CS1-I/O
T8	I/O
T7	I/O
N7	I/O
P7	I/O
R7	D2-I/O
T6	I/O
R6	I/O
N6	I/O
P6	I/O
T5	I/O
R5	D1-I/O
P5	RDY/BUSY-RCLK-I/O
N5	I/O
T4	I/O
R4	I/O
P4	I/O

PGA Pin Number	XC3090, XC3195
R3	D0-DIN-I/O
N4	DOUT-I/O
R2	CCLK
P3	VCC
N3	GND
P2	A0-WS-I/O
M3	A1-CS2-I/O
R1	I/O
N2	I/O
P1	A2-I/O
N1	A3-I/O
L3	I/O
M2	I/O
M1	A15-I/O
L2	A4-I/O
L1	I/O
K3	I/O
K2	A14-I/O
K1	A5-I/O
J1	I/O
J2	I/O
J3	GND
H3	VCC
H2	A13-I/O
H1	A6-I/O
G1	I/O
G2	I/O
G3	I/O
F1	I/O
F2	A12-I/O
E1	A7-I/O
E2	I/O
F3	I/O
D1	A11-I/O
C1	A8-I/O
D2	I/O
B1	I/O
E3	A10-I/O
C2	A9-I/O
D3	VCC
C3	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

Pins A2, A3, A15, A16, T1, T2, T3, T15 and T16 are not connected. Pin A1 does not exist.

XC3090 176-Pin TQFP Pinouts

XC3000, XC3000A, XC3000L, XC3100 and XC3100A families have identical pinouts

Pin Number	XC3090	Pin Number	XC3090	Pin Number	XC3090	Pin Number	XC3090
1	PWRDWN	45	M1-RDATA	89	DONE-PG	133	VCC
2	TCLKIN-I/O	46	GND	90	D7-I/O	134	GND
3	I/O	47	M0-RTRIG	91	XTAL1(OUT)-BCLKIN-I/O	135	A0-WS-I/O
4	I/O	48	VCC	92	I/O	136	A1-CS2-I/O
5	I/O	49	M2-I/O	93	I/O	137	-
6	I/O	50	HDC-I/O	94	I/O	138	I/O
7	I/O	51	I/O	95	I/O	139	I/O
8	I/O	52	I/O	96	D6-I/O	140	A2-I/O
9	I/O	53	I/O	97	I/O	141	A3-I/O
10	I/O	54	LDC-I/O	98	I/O	142	-
11	I/O	55	-	99	I/O	143	-
12	I/O	56	I/O	100	I/O	144	I/O
13	I/O	57	I/O	101	I/O	145	I/O
14	I/O	58	I/O	102	D5-I/O	146	A15-I/O
15	I/O	59	I/O	103	CS0-I/O	147	A4-I/O
16	I/O	60	I/O	104	I/O	148	I/O
17	I/O	61	I/O	105	I/O	149	I/O
18	I/O	62	I/O	106	I/O	150	A14-I/O
19	I/O	63	I/O	107	I/O	151	A5-I/O
20	I/O	64	I/O	108	D4-I/O	152	I/O
21	I/O	65	INIT-I/O	109	I/O	153	I/O
22	GND	66	VCC	110	VCC	154	GND
23	VCC	67	GND	111	GND	155	VCC
24	I/O	68	I/O	112	D3-I/O	156	A13-I/O
25	I/O	69	I/O	113	CS1-I/O	157	A6-I/O
26	I/O	70	I/O	114	I/O	158	I/O
27	I/O	71	I/O	115	I/O	159	I/O
28	I/O	72	I/O	116	I/O	160	-
29	I/O	73	I/O	117	I/O	161	-
30	I/O	74	I/O	118	D2-I/O	162	I/O
31	I/O	75	I/O	119	I/O	163	I/O
32	I/O	76	I/O	120	I/O	164	A12-I/O
33	I/O	77	I/O	121	I/O	165	A7-I/O
34	I/O	78	I/O	122	I/O	166	I/O
35	I/O	79	I/O	123	I/O	167	I/O
36	I/O	80	I/O	124	D1-I/O	168	-
37	I/O	81	I/O	125	RDY/BUSY-RCLK-I/O	169	A11-I/O
38	I/O	82	-	126	I/O	170	A8-I/O
39	I/O	83	-	127	I/O	171	I/O
40	I/O	84	I/O	128	I/O	172	I/O
41	I/O	85	XTAL2(IN)-I/O	129	I/O	173	A10-I/O
42	I/O	86	GND	130	D0-DIN-I/O	174	A9-I/O
43	I/O	87	RESET	131	DOUT-I/O	175	VCC
44	-	88	VCC	132	CCLK	176	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

XC3090 208-Pin PQFP Pinouts

XC3000, XC3000A, XC3000L, XC3100 and XC3100A families have identical pinouts

Pin Number	XC3090	Pin Number	XC3090	Pin Number	XC3090	Pin Number	XC3090
1	–	53	–	105	–	157	–
2	**GND**	54	–	106	**VCC**	158	–
3	PWRDWN	55	**VCC**	107	D/P	159	–
4	TCLKIN-I/O	56	M2-I/O	108	–	160	**GND**
5	I/O	57	HDC-I/O	109	D7-I/O	161	WS-A0-I/O
6	I/O	58	I/O	110	XTL1-BCLKIN-I/O	162	CS2-A1-I/O
7	I/O	59	I/O	111	I/O	163	I/O
8	I/O	60	I/O	112	I/O	164	I/O
9	I/O	61	LDC-I/O	113	I/O	165	A2-I/O
10	I/O	62	I/O	114	I/O	166	A3-I/O
11	I/O	63	I/O	115	D6-I/O	167	I/O
12	I/O	64	–	116	I/O	168	I/O
13	I/O	65	–	117	I/O	169	–
14	I/O	66	–	118	I/O	170	–
15	–	67	–	119	–	171	–
16	I/O	68	I/O	120	I/O	172	A15-I/O
17	I/O	69	I/O	121	I/O	173	A4-I/O
18	I/O	70	I/O	122	D5-I/O	174	I/O
19	I/O	71	I/O	123	CS0-I/O	175	I/O
20	I/O	72	–	124	I/O	176	–
21	I/O	73	–	125	I/O	177	–
22	I/O	74	I/O	126	I/O	178	A14-I/O
23	I/O	75	I/O	127	I/O	179	A5-I/O
24	I/O	76	I/O	128	D4-I/O	180	I/O
25	**GND**	77	INIT-I/O	129	I/O	181	I/O
26	**VCC**	78	**VCC**	130	**VCC**	182	**GND**
27	I/O	79	**GND**	131	**GND**	183	**VCC**
28	I/O	80	I/O	132	D3-I/O	184	A13-I/O
29	I/O	81	I/O	133	CS1-I/O	185	A6-I/O
30	I/O	82	I/O	134	I/O	186	I/O
31	I/O	83	–	135	I/O	187	I/O
32	I/O	84	–	136	I/O	188	–
33	I/O	85	I/O	137	I/O	189	–
34	I/O	86	I/O	138	D2-I/O	190	I/O
35	I/O	87	I/O	139	I/O	191	I/O
36	I/O	88	I/O	140	I/O	192	A12-I/O
37	–	89	I/O	141	I/O	193	A7-I/O
38	I/O	90	–	142	–	194	–
39	I/O	91	–	143	I/O	195	–
40	I/O	92	–	144	I/O	196	–
41	I/O	93	I/O	145	D1-I/O	197	I/O
42	I/O	94	I/O	146	RDY/BUSY-RCLK-I/O	198	I/O
43	I/O	95	I/O	147	I/O	199	A11-I/O
44	I/O	96	I/O	148	I/O	200	A8-I/O
45	I/O	97	I/O	149	I/O	201	I/O
46	I/O	98	I/O	150	I/O	202	I/O
47	I/O	99	I/O	151	DIN-D0-I/O	203	A10-I/O
48	M1-RDATA	100	XTL2-I/O	152	DOUT-I/O	204	A9-I/O
49	**GND**	101	**GND**	153	CCLK	205	**VCC**
50	M0-RTRIG	102	RESET	154	**VCC**	206	–
51	–	103	–	155	–	207	–
52	–	104	–	156	–	208	–

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

*In PQ208, XC3090 and XC3195 have different pinouts.

XC3195 PQ208 and PG223 Pinouts

Pin Description	PG223	PQ208 *
A9-I/O	B1	206
A10-I/O	E3	205
I/O	E4	204
I/O	C2	203
I/O	C1	202
I/O	D2	201
A8-I/O	E2	200
A11-I/O	F4	199
I/O	F3	198
I/O	D1	197
I/O	F2	196
I/O	G2	194
A7-I/O	G4	193
A12-I/O	G1	192
I/O	H2	191
I/O	H3	190
I/O	H1	189
I/O	H4	188
I/O	J3	187
I/O	J2	186
A6-I/O	J1	185
A13-I/O	K3	184
VCC	J4	183
GND	K4	182
I/O	K2	181
I/O	K1	180
A5-I/O	L2	179
A14-I/O	L4	178
I/O	L3	177
I/O	L1	176
I/O	M1	175
I/O	M2	174
A4-I/O	M4	173
A15-I/O	N2	172
I/O	N3	171
I/O	P2	169
I/O	R1	168
I/O	N4	167
A3-I/O	T1	166
A2-I/O	R2	165
I/O	P3	164
I/O	T2	163
I/O	P4	162
I/O	U1	161
A1-CS2-I/O	V1	160
A0-$\overline{WS}$-I/O	T3	159
GND	R3	158
VCC	R4	157
CCLK	U2	156
DOUT-I/O	V2	155

Pin Description	PG223	PQ208 *
D0-DIN-I/O	U3	154
I/O	V3	153
I/O	R5	152
I/O	T4	151
I/O	V4	150
RDY/$\overline{BUSY}$-RCLK-I/O	U4	149
D1-I/O	U5	148
I/O	R6	147
I/O	T5	146
I/O	U6	145
I/O	T6	144
I/O	V7	141
I/O	R7	140
I/O	U7	139
D2-I/O	V8	138
I/O	U8	137
I/O	T8	136
I/O	R8	135
I/O	V9	134
$\overline{CS1}$-I/O	U9	133
D3-I/O	T9	132
GND	R9	131
VCC	R10	130
I/O	T10	129
D4-I/O	U10	128
I/O	V10	127
I/O	R11	126
I/O	T11	125
I/O	U11	124
$\overline{CS0}$-I/O	V11	123
D5-I/O	U12	122
I/O	R12	121
I/O	V12	120
I/O	T13	119
I/O	U13	118
I/O	T14	117
I/O	R13	116
I/O	U14	115
D6-I/O	U15	114
I/O	V15	113
I/O	T15	112
I/O	R14	111
I/O	V16	110
XTL1(OUT)BCLKIN-I/O	U16	109
D7-I/O	T16	108
D/$\overline{P}$	V17	107
VCC	R15	106
$\overline{RESET}$	U17	105
GND	R16	104
XTL2(IN)-I/O	V18	103

Pin Description	PG223	PQ208 *
I/O	U18	102
I/O	P15	101
I/O	T17	100
I/O	T18	99
I/O	P16	98
I/O	R17	97
I/O	N15	96
I/O	R18	95
I/O	P17	94
I/O	N17	93
I/O	N16	92
I/O	M15	89
I/O	M18	88
I/O	M17	87
I/O	L18	86
I/O	L17	85
I/O	L15	84
I/O	L16	83
I/O	K18	82
I/O	K17	81
I/O	K16	80
GND	K15	79
VCC	J15	78
$\overline{INIT}$	J16	77
I/O	J17	76
I/O	J18	75
I/O	H16	74
I/O	H15	73
I/O	H17	72
I/O	H18	71
I/O	G17	70
I/O	G18	69
I/O	G15	68
I/O	F16	67
I/O	F17	66
I/O	E17	63
I/O	C18	62
I/O	F15	61
I/O	D17	60
$\overline{LDC}$-I/O	E16	59
I/O	C17	58
I/O	B18	57
I/O	E15	56
HDC-I/O	A18	55
M2-I/O	A17	54
VCC	D16	53
M0-RTIG	B17	52
GND	D15	51
M1/$\overline{RDATA}$	C16	50

Pin Description	PG223	PQ208 *
I/O	B16	49
I/O	A16	48
I/O	D14	47
I/O	C15	46
I/O	B15	45
I/O	A15	44
I/O	C14	43
I/O	D13	42
I/O	B14	41
I/O	C13	40
I/O	B13	39
I/O	B12	38
I/O	D12	37
I/O	A12	36
I/O	B11	35
I/O	C11	34
I/O	A11	33
I/O	D11	32
I/O	A10	31
I/O	B10	30
I/O	C10	29
I/O	C9	28
VCC	D10	27
GND	D9	26
I/O	B9	25
I/O	A9	24
I/O	C8	23
I/O	D8	22
I/O	B8	21
I/O	A8	20
I/O	B7	19
I/O	A7	18
I/O	D7	17
I/O	B6	14
I/O	C6	13
I/O	B5	12
I/O	A4	11
I/O	D6	10
I/O	C5	9
I/O	B4	8
I/O	B3	7
I/O	C4	6
I/O	D5	5
I/O	C3	4
I/O	A3	3
TCLKIN-I/O	A2	2
$\overline{PWRDN}$	B2	1
GND	D4	208
VCC	D3	207

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

In the PQ208 package, pins 15, 16, 64, 65, 90, 91, 142, 143, 170 and 195 are not connected.

*In PQ208, XC3090 and XC3195 have different pinouts.

XC3000 Component Availability

PINS		44	64	68	84		100				132		144	160	164	175		176	208	223
TYPE		PLAST. PLCC	PLAST. VQFP	PLAST. PLCC	PLAST. PLCC	CERAM PGA	PLAST. PQFP	PLAST. TQFP	PLAST. VQFP	TOP-BRAZED CQFP	PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	TOP-BRAZED CQFP	PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	CERAM. PGA
CODE		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	CB100	PP132	PG132	TQ144	PQ160	CB164	PP175	PG175	TQ176	PQ208	PG223
XC3020	-50					MB				MB										
	-70			CI	CI	CIMB	CI			CMB										
	-100			CI	CI	CIMB	CI			CMB										
	-125			C	C	C	C													
XC3030	-50					M														
	-70	CI		CI	CI	CIM	CI	C												
	-100	CI		CI	CI	CIM	CI	C												
	-125	C		C	C	C	C	C												
XC3042	-50					MB				MB		MB								
	-70				CI	CIMB	CI	C		CMB	C	CIMB								
	-100				CI	CIMB	CI	C		CMB	C	CIMB								
	-125				C	C	C	C			C	C								
XC3064	-50											M								
	-70				CI						CI	CIM		CI						
	-100				CI						CI	CIM		CI						
	-125				C						C	C		C						
XC3090	-50														MB		MB			
	-70				CI									CI	CIMB	CI	CIMB		CI	
	-100				CI									CI	CIMB	CI	CIMB		CI	
	-125				C									C		C	C		C	
XC3020A	-7			CI	CI	CI	CI													
	-6			C	C	C	C													
XC3030A	-7	CI	CI	CI	CI	CI	CI		CI											
	-6	C	C	C	C	C	C		C											
XC3042A	-7				CI	CI	CI		CI		CI	CI	CI							
	-6				C	C	C		C		C	C	C							
XC3064A	-7				CI						CI	CI	CI	CI						
	-8				C						C	C	C	C						
XC3090A	-7				CI									CI		CI	CI	CI	CI	
	-8				C									C		C	C	C	C	
XC3020L					C															
XC3030L			C		C				C											
XC3042L					C				C				C							
XC3064L					C								C							
XC3090L					C													C		
XC3120A	-5			CI	CI	CI	CI													
	-4			CI	CI	CI	CI													
	-3			CI	CI	CI	CI													
	-2			CI	CI	CI	CI													
	-1			CI	CI	CI	CI													
XC3130A	-5	CI	CI	CI	CI	CI	CI	C												
	-4	CI	CI	CI	CI	CI	CI	C												
	-3	CI	CI	CI	CI	CI	CI	CI												
	-2	CI	CI	CI	CI	CI	CI	CI												
	-1	C	C	C	C	C	C	C												
XC3142A	-5				CI	CIMB	CI	C		MB	C	CIMB	CI							
	-4				CI	CI	CI	C			C	CI	CI							
	-3				CI	CI	CI	CI			CI	CI	CI							
	-2				CI	CI	CI	CI			CI	CI	CI							
	-1				C	C	C	C			C	C	C							
XC3164A	-5				CI						CI	CI	CI	CI						
	-4				CI						CI	CI	CI	CI						
	-3				CI						CI	CI	CI	CI						
	-2				CI						CI	CI	CI	CI						
	-1				C						C	C	C	C						
XC3190A	-5				CI									CI	MB	CI	CIMB	CI	CI	
	-4				CI									CI		CI	CI	CI	CI	
	-3				CI									CI		CI	CI	CI	CI	
	-2				CI									CI		CI	CI	CI	CI	
	-1				C									C		C	C	C	C	
XC3195A	-5				CI									CI	MB	CI	CIMB		CI	CI
	-4				CI									CI		CI	CI		CI	CI
	-3				CI									CI		CI	CI		CI	CI
	-2				CI									CI		CI	CI		CI	CI
	-1				C									C		C	C		C	C

C = Commercial = 0° to +85° C I = Industrial = -40° to +100° C M = Mil Temp = -55° to +125° C B = MIL-STD-883C Class B

Parentheses indicate future product plans

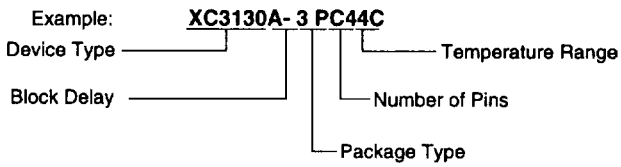
For a detailed description of the device architecture, see pages 2-105 through 2-123.

For a detailed description of the configuration modes and their timing, see pages 2-124 through 2-132.

For detailed lists of package pin-outs, see pages 2-140 through 2-150.

For package physical dimensions and thermal data, see Section 4.

Ordering Information



XC3000, XC3000A, XC3000L, XC3100, XC3100A

The features of the original **XC3000** family are described on the preceding pages.

XC3100A is functionally identical with XC3000, but offers substantially faster performance. There is also an additional high-end family member, the XC3195A.

XC3000L uses a 3.3 V supply voltage and has lower power-down current.

The **XC3000A, XC3000L** and **XC3100A** families all offer identical enhanced functionality. They are thus supersets of the XC3000 familiy.

Additional routing resources provide improved performance and higher density. There is now a direct connection from each CLB output to the data input of its nearest TBUF. This speeds up the path and preserves general routing resources that can be used for other purposes.

The **CLB clock enable and the TBUF output enable** are now driven by two different vertical Longlines. In the XC3000/3100 devices, the CLB clock enable signal and the adjacent TBUF output enable signal can both be driven only from the same vertical Longline. That makes these two functions mutually exclusive, and thus creates placement constraints. Using separate Longlines for these two functions leads to improved density and performance, especially in bus-oriented applications.

Bitstream error checking protects against erroneous configuration.

Each Xilinx FPGA bitstream consists of a 40-bit preamble, followed by a device-specific number of data frames. The number of bits per frame is also device-specific; however, each frame ends with three stop bits (111) followed by a start bit for the next frame (0).

All devices in all XC3000 families start reading in a new frame when they find the first 0 after the end of the previous frame. XC3000/XC3100 devices do not check for the correct stop bits, but XC3000A/XC3100A and XC3000L devices check that the last three bits of any frame are actually 111.

Under normal circumstances, all these FPGAs behave the same way; however, if the bitstream is corrupted, an XC3000/XC3100 device will always start a new frame as soon as it finds the first 0 after the end of the previous frame, even if the data is completely wrong or out-of-sync. Given sufficient zeros in the data stream, the device will also go Done, but with incorrect configuration and the possibility of internal contention.

An XC3000A/XC3100A/XC3000L device starts any new frame only if the three preceding bits are all ones. If this check fails, it pulls $\overline{\text{INIT}}$ Low and stops the internal configuration, although the Master CCLK keeps running. The user must then start a new configuration by applying a >6 µs Low level on $\overline{\text{RESET}}$.

This simple check does not protect against random bit errors, but it offers almost 100 percent protection against erroneous configuration files, defective configuration data sources, synchronization errors between configuration source and FPGA, or PC-board level defects, such as broken lines or solder-bridges.

A separate modification slows down the $\overline{\text{RESET}}$ input before configuration by using a two-stage shift register driven from the internal clock. It tolerates submicrosecond High spikes on $\overline{\text{RESET}}$ before configuration. The XC3000 master can be connected like an XC4000 master, but with its $\overline{\text{RESET}}$ input used instead of $\overline{\text{INIT}}$. (On XC3000, $\overline{\text{INIT}}$ is output only).

Soft start-up. After configuration, the outputs of all LCA device in a daisy-chain become active simultaneously, as a result of the same CCLK edge. In the original XC3000/3100 devices, each output becomes active in either fast or slew-rate limited mode, depending on the way it is configured. This can lead to large ground-bounce signals. In the new XC3000A/XC3000L/XC31000A devices, all outputs become active first in slew-rate limited mode, reducing the ground bounce. After this soft start-up, each individual output slew rate is again controlled by the respective configuration bit.

The XC3000, XC3000L, ZC3100A are fully supported by the XACT Version 5.0, or later, development system. XACT 5.0 provides many advanced features not available with the XC3000 software such as timing-driven place and route (XACT-Performance™)and the X-BLOX™ module generator.

IMPORTANT NOTICE
All new designs should use XC3000A. Information on XC3000 is presented here as a reference for existing designs. XC3000 bitstreams are upward compatible to XC3000A without modification.

XC3000
Logic Cell Array Family

Product Specification

Features

- Industry-leading FPGA family with five device types
  - Logic densities from 1,000 to 6,000 gates
  - Up to 144 user-definable I/Os
- Guaranteed 70- to 125-MHz toggle rates, 9 to 5.5 ns logic delays
- Advanced CMOS static memory technology
  - Low quiescent and active power consumption
- XC3000-specific features
  - Ultra-low current option in Power-Down mode
  - 4-mA output sink and source current
  - Broad range of package options includes plastic and ceramic quad flat packs, plastic leaded chip carriers and pin grid arrays
  - 100% bitstream compatible with the XC3100 family
  - Commercial, industrial, military, "high rel", and MIL-STD-883 Class B grade devices
  - Easy migration to XC3300 series of HardWire mask-programmed devices for high-volume production

Description

XC3000 is the original family of devices in the XC3000 class of Field Programmable Gate Array (FPGA) architectures. The XC3000 family has a proven track record in addressing a wide range of design applications, including general logic replacement and sub-systems integration. For a thorough description of the XC3000 architecture see the preceding pages of this data book.

The XC3000 Family covers a range of nominal device densities from 2,000 to 9,000 gates, practically achievable densities from 1,000 to 6,000 gates. Device speeds, described in terms of maximum guaranteed toggle frequencies, range from 70 to 125 MHz. The performance of a completed design depends upon placement and routing implementation, so, like with any gate array, the final verification of device utilization and performance can only be known after the design has been placed and routed.

Device	CLBs	Array	User I/Os Max	Flip-Flops	Horizontal Longlines	Configuration Data Bits
XC3020	64	8 x 8	64	256	16	14,779
XC3030	100	10 x 10	80	360	20	22,176
XC3042	144	12 x 12	96	480	24	30,784
XC3064	224	16 x 14	120	688	32	46,064
XC3090	320	16 x 20	144	928	40	64,160

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	−0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	−0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	−0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	−65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial -40°C to +100°C junction	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration	2.0	V_{CC}	V
V_{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration	70%	100%	V_{CC}
V_{ILC}	Low-level input voltage — CMOS configuration	0	20%	V_{CC}
T_{IN}	Input signal transition time		250	ns

At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.

DC Characteristics Over Operating Conditions

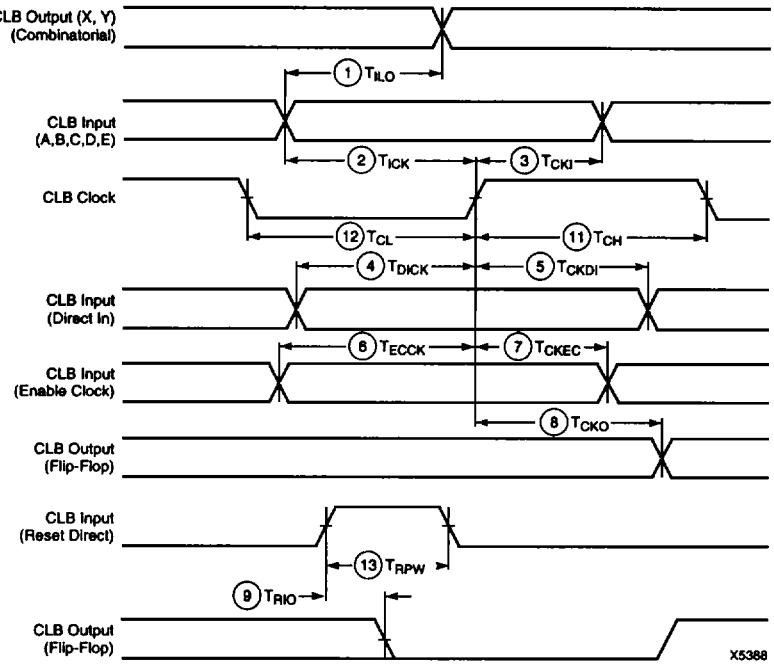
Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	Commercial	3.86		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)			0.40	V
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	Industrial	3.76		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)			0.40	V
V_{CCPD}	Power-down supply voltage ($\overline{PWRDWN}$ must be Low)		2.30		V
I_{CCPD}	Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX})[1]	XC3020		50	µA
		XC3030		80	µA
		XC3042		120	µA
		XC3064		170	µA
		XC3090		250	µA
I_{CCO}	Quiescent LCA supply current in addition to I_{CCPD}[2] Chip thresholds programmed as CMOS levels			500	µA
	Chip thresholds programmed as TTL levels			10	mA
I_{IL}	Input Leakage Current		–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 10 15	 pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 15 20	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V (sample tested)		0.02	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low			3.4	mA

Note: 1. Devices with much lower I_{CCPD} tested and guaranteed at V_{CC} = 3.2 V, T = 25°C can be ordered with a Special Product Code.

XC3020 SPC0107: I_{CCPD} = 1 µA
XC3030 SPC0107: I_{CCPD} = 2 µA
XC3042 SPC0107: I_{CCPD} = 3 µA
XC3064 SPC0107: I_{CCPD}= 4 µA
XC3090 SPC0107: I_{CCPD}= 5 µA

2. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the LCA configured with a MakeBits tie option.

CLB Switching Characteristic Guidelines



Buffer (Internal) Switching Characteristic Guidelines

	Speed Grade	-70	-100	-125	Units
Description	**Symbol**	**Max**	**Max**	**Max**	
Global and Alternate Clock Distribution*					
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	8.0	7.5	7.0	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	6.5	6.0	5.7	ns
TBUF driving a Horizontal Longline (L.L.)*					
I to L.L. while T is Low (buffer active)	T_{IO}	5.0	4.7	4.5	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	11.0	10.0	9.0	ns
T↓ to L.L. active and valid with pair of pull-up resistors	T_{ON}	12.0	11.0	10.0	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	24.0	22.0	17.0	ns
T↑ to L.L. High with pair of pull-up resistors	T_{PUF}	17.0	15.0	12.0	ns
BIDI					
Bidirectional buffer delay	T_{BIDI}	2.0	1.8	1.7	ns

* Timing is based on the XC3042, for other devices see XACT timing calculator.

CLB Switching Characteristic Guidelines (continued)

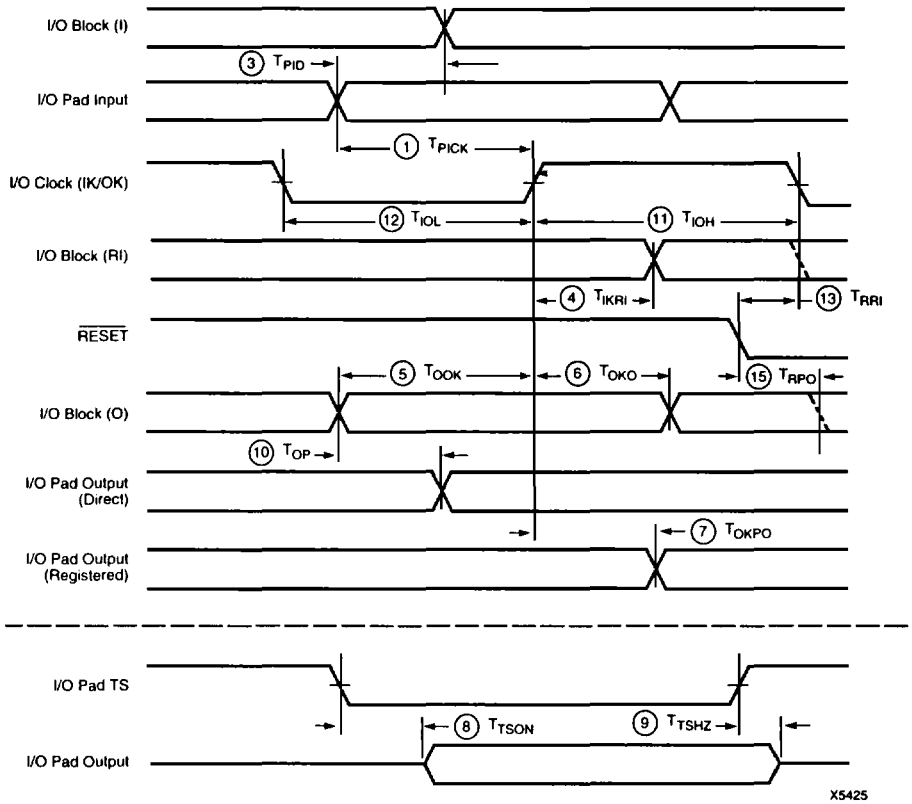
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

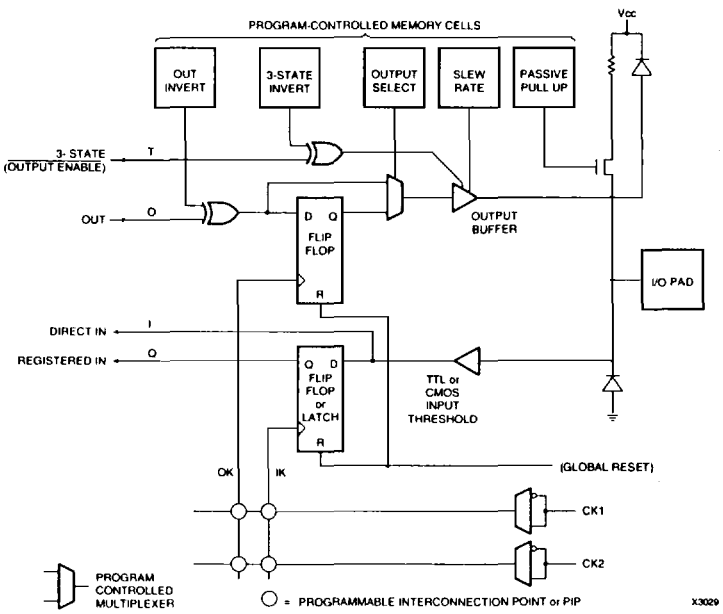
Speed Grade			-70		-100		-125		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delay									
Logic Variables A, B, C, D, E, to outputs X or Y	1	T_{ILO}		9.0		7.0		5.5	ns
Sequential delay									
Clock k to outputs X or Y	8	T_{CKO}		6.0		5.0		4.5	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y		T_{QLO}		13.0		10.0		8.0	ns
Set-up time before clock K									
Logic Variables A, B, C, D, E	2	T_{ICK}	8.0		7.0		5.5		ns
Data In DI	4	T_{DICK}	5.0		4.0		3.0		ns
Enable Clock EC	6	T_{ECCK}	7.0		5.0		4.5		ns
Reset Direct inactive RD			1.0		1.0		1.0		ns
Hold Time after clock K									
Logic Variables A, B, C, D, E	3	T_{CKI}	0		0		0		ns
Data In DI	5	T_{CKDI}	4.0		2.0		1.5		ns
Enable Clock EC	7	T_{CKEC}	0		0		0		ns
Clock									
Clock High time	11	T_{CH}	5.0		4.0		3.0		ns
Clock Low time	12	T_{CL}	5.0		4.0		3.0		ns
Max flip-flop toggle rate		F_{CLK}	70		100		125		MHz
Reset Direct (RD)									
RD width	13	T_{RPW}	8.0		7.0		6.0		ns
delay from rd to outputs X or Y	9	T_{RIO}		8.0		7.0		6.0	ns
Global Reset ($\overline{\text{RESET}}$ Pad)*									
$\overline{\text{RESET}}$ width (Low)		T_{MRW}	25.0		21.0		20.0		ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y		T_{MRQ}		23.0		19.0		17.0	ns

*Timing is based on the XC3042, for other devices see XACT timing calculator.

Note: The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

IOB Switching Characteristic Guidelines





IOB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade		-70		-100		-125		Units
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Propagation Delays (Input)									
Pad to Direct In (I)	3	T_{PID}		6		4		3	ns
Pad to Registered In (Q) with latch transparent		T_{PTG}		21		17		16	ns
Clock (IK) to Registered In (Q)	4	T_{IKRI}		5.5		4		3	ns
Set-up Time (Input)									
Pad to Clock (IK) set-up time	1	T_{PICK}	20		17		16		ns
Propagation Delays (Output)									
Clock (OK) to Pad (fast)	7	T_{OKPO}		13		10		9	ns
same (slew rate limited)	7	T_{OKPO}		33		27		24	ns
Output (O) to Pad (fast)	10	T_{OPF}		9		6		5	ns
same (slew-rate limited)	10	T_{OPS}		29		23		20	ns
3-state to Pad begin hi-Z (fast)	9	T_{TSHZ}		8		8		7	ns
same (slew-rate limited)	9	T_{TSHZ}		28		25		24	ns
3-state to Pad active and valid (fast)	8	T_{TSON}		14		12		11	ns
same (slew -rate limited)	8	T_{TSON}		34		29		27	ns
Set-up and Hold Times (Output)									
Output (O) to clock (OK) set-up time	5	T_{OOK}	10		9		8		ns
Output (O) to clock (OK) hold time	6	T_{OKO}	0		0		0		ns
Clock									
Clock High time	11	T_{IOH}	5		4		3		ns
Clock Low time	12	T_{IOL}	5		4		3		ns
Max. flip-flop toggle rate		F_{CLK}	70		100		125		MHz
Global Reset Delays (based on XC3042)									
$\overline{\text{RESET}}$ Pad to Registered In (Q)	13	T_{RRI}		25		24		23	ns
$\overline{\text{RESET}}$ Pad to output pad (fast)	15	T_{RPO}		35		33		29	ns
(slew-rate limited)	15	T_{RPO}		53		45		42	ns

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). For larger capacitive loads, see XAPP 024. Typical slew rate limited output rise/fall times are approximately four times longer.

2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.

3. Input pad setup time and hold times are specified with respect to the internal clock (IK). To calculate system setup time, subtract clock delay (clock pad to IK) from the specified input pad setup time value, but the subtracted value cannot be less than zero (i.e., negative hold time). Negative hold time means that the delay in the input data is adequate for the **external system hold time** to be zero, provided the input clock uses the Global signal distribution from pad to IK .

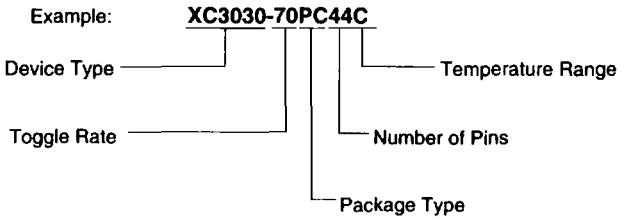
For a detailed description of the device architecture, see pages 2-105 through 2-123.

For a detailed description of the configuration modes and their timing, see pages 2-124 through 2-132.

For detailed lists of package pin-outs, see pages 2-140 through 2-150.

For package physical dimensions and thermal data, see Section 4.

Ordering Information



Component Availability

PINS		44	64	68	84		100				132		144	160	164	175		176	208	223
TYPE		PLAST. PLCC	PLAST. VQFP	PLAST. PLCC	PLAST. PLCC	CERAM. PGA	PLAST. PQFP	PLAST. TQFP	PLAST. VQFP	TOP-BRAZED CQFP	PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	TOP-BRAZED CQFP	PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	CERAM. PGA
CODE		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	CB100	PP132	PG132	TQ144	PQ160	CB164	PP175	PG175	TQ176	PQ208	PG223
XC3020	-50					MB				MB										
	-70			CI	CI	CIMB	CI			CMB										
	-100			CI	CI	CIMB	CI			CMB										
	-125			C	C	C	C													
XC3030	-50					M														
	-70	CI		CI	CI	CIM	CI	C												
	-100	CI		CI	CI	CIM	CI	C												
	-125	C		C	C	C	C	C												
XC3042	-50					MB				MB		MB								
	-70				CI	CIMB	CI	C		CMB	C	CIMB								
	-100				CI	CIMB	CI	C		CMB	C	CIMB								
	-125				C	C	C	C			C	C								
XC3064	-50											M								
	-70				CI						CI	CIM		CI						
	-100				CI						CI	CIM		CI						
	-125				C						C	C		C						
XC3090	-50														MB		MB			
	-70				CI									CI	CMB	CI	CIMB		CI	
	-100				CI									CI	CMB	CI	CIMB		CI	
	-125				C									C		C	C		C	

C = Commercial = 0° to +70° C I = Industrial = -40° to +85° C M = Mil Temp = -55° to +125° C B = MIL-STD-883C Class B

Parentheses indicate future product plans

XC3000A
Logic Cell Array Family

Product Specifications

Features

- Enhanced, high performance FPGA family with five device types
  - Improved redesign of the basic XC3000 LCA Family
  - Logic densities from 1,000 to 6,000 gates
  - Up to 144 user-definable I/Os
- Superset of the industry-leading XC3000 family
  - Identical to the basic XC3000 in structure, pin out, design methodology, and software tools
  - 100% compatible with all XC3000, XC3000L, and XC3100 bitstreams
  - Improved routing and additional features
- Additional programmable interconnection points (PIPs)
  - Improved access to longlines and CLB clock enable inputs
  - Most efficient XC3000-class solution to bus-oriented designs
- Advanced 0.8 µ CMOS static memory technology
  - Low quiescent and active power consumption
- Performance specified by logic delays, faster than corresponding XC3000 versions
- XC3000A-specific features
  - 4 mA output sink and source current
  - Error checking of the configuration bitstream
  - Soft startup starts all outputs in slew-limited mode upon power-up
  - Easy migration to the XC3400 series of HardWire mask programmed devices for high-volume production.

Description

The XC3000A family offers the following enhancements over the popular XC3000 family:

The XC3000A family has additional interconnect resources to drive the I-inputs of TBUFs driving horizontal Longlines. The CLB Clock Enable input can be driven from a second vertical Longline. These two additions result in more efficient and faster designs when horizontal Longlines are used for data bussing.

During configuration, the XC3000A devices check the bitstream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls INIT Low.

When the configuration process is finished and the device starts up in user mode, the first activation of the outputs is automatically slew-rate limited . This feature, called Soft Startup, avoids the potential ground bounce when all outputs are turned on simultaneously. After start-up, the slew rate of the individual outputs is, as in the XC3000 family, determined by the individual configuration option.

The XC3000A family is a superset of the XC3000 family. Any bitstream used to configure an XC3000 or XC3100 device configures an XC3000A device exactly the same way.

Device	CLBs	Array	User I/Os Max	Flip-Flops	Horizontal Longlines	Configurable Data Bits
XC3020A	64	8 x 8	64	256	16	14,779
XC3030A	100	10 x 10	80	360	20	22,176
XC3042A	144	12 x 12	96	480	24	30,784
XC3064A	224	16 x 14	120	688	32	46,064
XC3090A	320	16 x 20	144	928	40	64,160

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to Vcc +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to Vcc +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial -40°C to +100°C junction	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration	2.0	Vcc	V
V_{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration	70%	100%	V_{CC}
V_{ILC}	Low-level input voltage — CMOS configuration	0	20%	V_{CC}
T_{IN}	Input signal transition time		250	ns

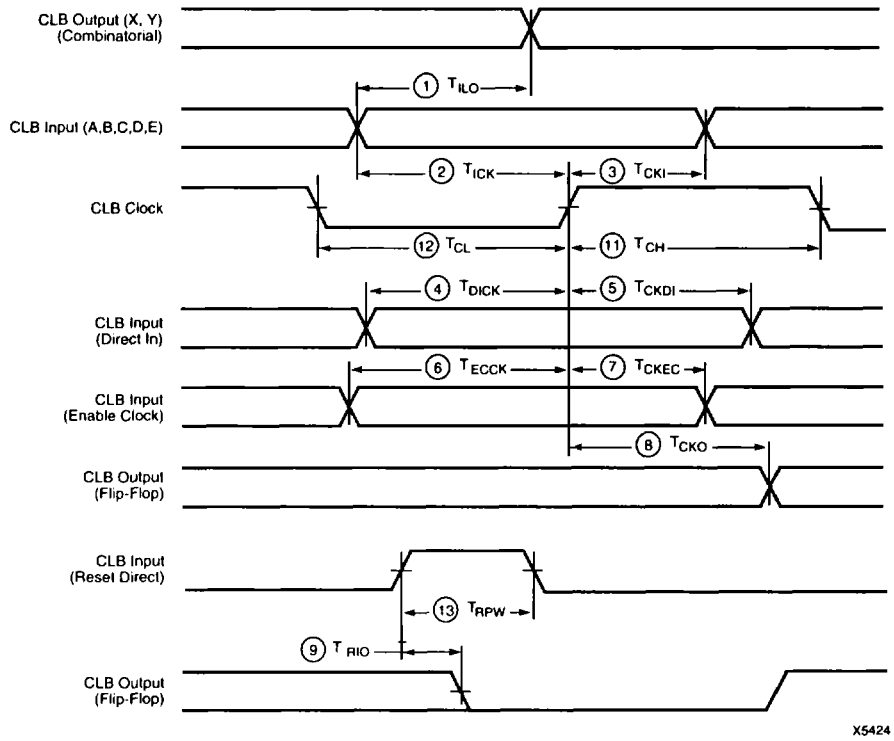
At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.

DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	Commercial	3.86		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)			0.40	V
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	Industrial	3.76		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)			0.40	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)		2.30		V
I_{CCPD}	Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX})			50	µA
I_{CCO}	Quiescent LCA supply current in addition to I_{CCPD}* Chip thresholds programmed as CMOS levels			500	µA
	Chip thresholds programmed as TTL levels			10	mA
I_{IL}	Input Leakage Current		–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 10 15	 pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 15 20	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V (sample tested)		0.02	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low			3.4	mA

* With no output current loads, no active input or Longline pull-up resistors, all package pins at Vcc or GND, and the LCA device configured with a MakeBits tie option.

CLB Switching Characteristic Guidelines



Buffer (Internal) Switching Characteristic Guidelines

Description	Symbol	-7 Max	-6 Max		Units
	Speed Grade	-7	-6		
Global and Alternate Clock Distribution*					
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	7.5	7.0		ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	6.0	5.7		ns
TBUF driving a Horizontal Longline (L.L.)*					
I to L.L. while T is Low (buffer active)	T_{IO}	4.5	4.0		ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	9.0	8.0		ns
T↓ to L.L. active and valid with pair of pull-up resistors	T_{ON}	11.0	10.0		ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	16.0	14.0		ns
T↑ to L.L. High with pair of pull-up resistors	T_{PUF}	10.0	8.0		ns
BIDI Bidirectional buffer delay	T_{BIDI}	1.7	1.5		ns

* Timing is based on the XC3042A, for other devices see XACT timing calculator.

CLB Switching Characteristic Guidelines (continued)

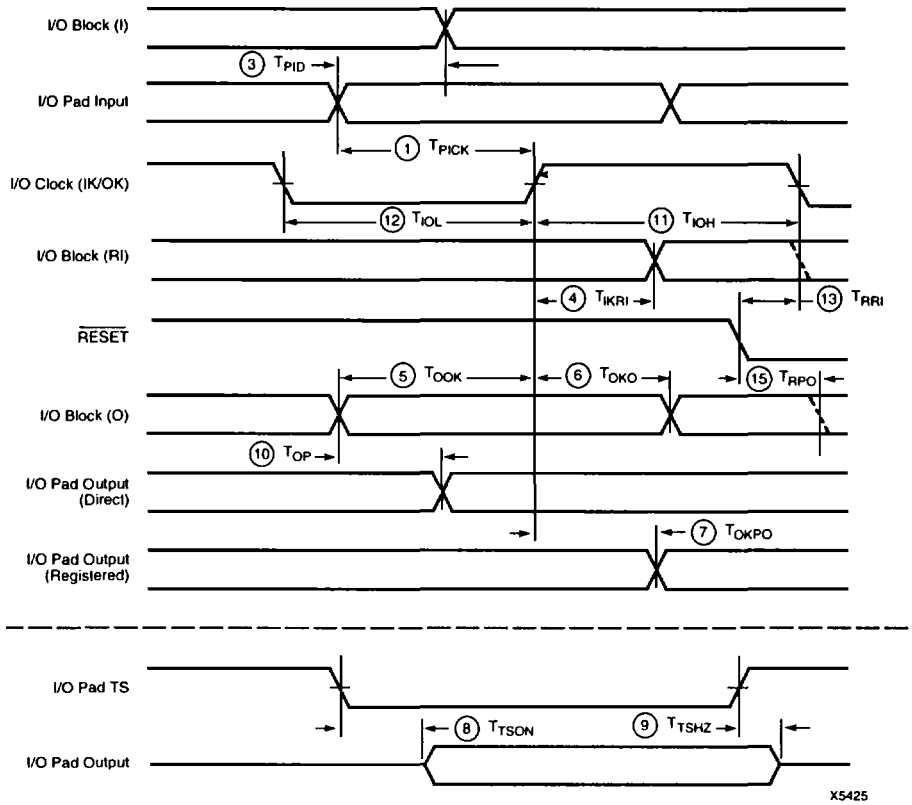
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

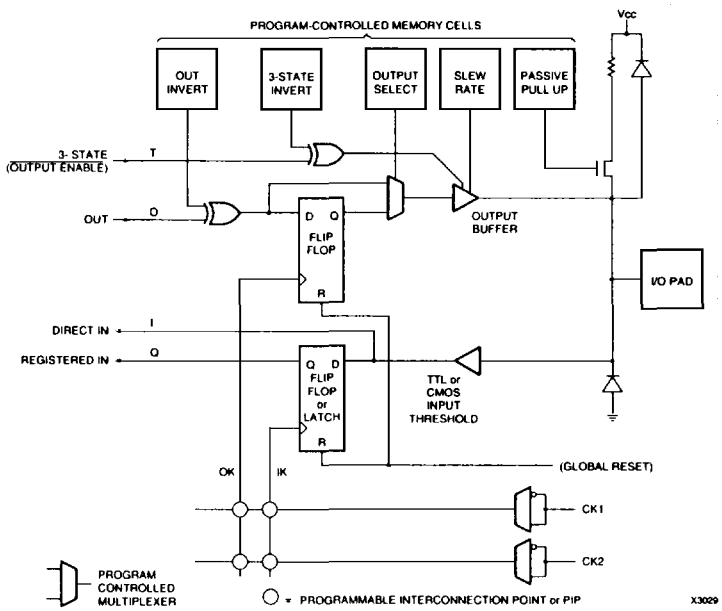
Description	Symbol		-7 Min	-7 Max	-6 Min	-6 Max	Units
Combinatorial Delay							
Logic Variables A, B, C, D, E, to outputs X or Y							
FG Mode	1	T_{ILO}		5.1		4.1	ns
F and FGM Mode				5.6		4.6	ns
Sequential delay							
Clock k to outputs X or Y	8	T_{CKO}		4.5		4.0	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y							
FG Mode		T_{QLO}		9.5		8.0	ns
F and FGM Mode				10.0		8.5	ns
Set-up time before clock K							
Logic Variables A, B, C, D, E							
FG Mode	2	T_{ICK}	4.5		3.5		ns
F and FGM Mode			5.0		4.0		ns
Data In DI	4	T_{DICK}	4.0		3.0		ns
Enable Clock EC	6	T_{ECCK}	4.5		4.0		ns
Hold Time after clock K							
Logic Variables A, B, C, D, E	3	T_{CKI}	0		0		ns
Data In DI	5	T_{CKDI}	1.0		1.0		ns
Enable Clock EC	7	T_{CKEC}	2.0		2.0		ns
Clock							
Clock High time	11	T_{CH}	4.0		3.5		ns
Clock Low time	12	T_{CL}	4.0		3.5		ns
Max. flip-flop toggle rate		F_{CLK}	113.0		135.0		MHz
Reset Direct (RD)							
RD width	13	T_{RPW}	6.0		5.0		ns
delay from RD to outputs X or Y	9	T_{RIO}		6.0		5.0	ns
Global Reset (RESET Pad)*							
RESET width (Low)		T_{MRW}	16.0		14.0		ns
delay from RESET pad to outputs X or Y		T_{MRQ}		19.0		17.0	ns

*Timing is based on the XC3042A, for other devices see XACT timing calculator.

Notes: The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

IOB Switching Characteristic Guidelines





IOB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

Description		Symbol		-7 Min	-7 Max	-6 Min	-6 Max			Units
Speed Grade										
Propagation Delays (Input)										
Pad to Direct In (I)		3	T_{PID}		4.0		3.0			ns
Pad to Registered In (Q) with latch transparent			T_{PTG}		15.0		14.0			ns
Clock (IK) to Registered In (Q)		4	T_{IKRI}		3.0		2.5			ns
Set-up Time (Input)										
Pad to Clock (IK) set-up time		1	T_{PICK}	14.0		12.0				ns
Propagation Delays (Output)										
Clock (OK) to Pad	(fast)	7	T_{OKPO}		8.0		7.0			ns
same	(slew rate limited)	7	T_{OKPO}		18.0		15.0			ns
Output (O) to Pad	(fast)	10	T_{OPF}		6.0		5.0			ns
same	(slew-rate limited)	10	T_{OPS}		16.0		13.0			ns
3-state to Pad begin hi-Z	(fast)	9	T_{TSHZ}		10.0		9.0			ns
same	(slew-rate limited)	9	T_{TSHZ}		20.0		12.0			ns
3-state to Pad active and valid	(fast)	8	T_{TSON}		11.0		10.0			ns
same	(slew -rate limited)	8	T_{TSON}		21.0		18.0			ns
Set-up and Hold Times (Output)										
Output (O) to clock (OK) set-up time		5	T_{OOK}	8.0		7.0				ns
Output (O) to clock (OK) hold time		6	T_{OKO}	0		0				ns
Clock										
Clock High time		11	T_{IOH}	4.0		3.5				ns
Clock Low time		12	T_{IOL}	4.0		3.5				ns
Max. flip-flop toggle rate			F_{CLK}	113.0		135.0				MHz
Global Reset Delays (based on XC3042A)										
$\overline{\text{RESET}}$ Pad to Registered In (Q)		13	T_{RRI}		24.0		23.0			ns
$\overline{\text{RESET}}$ Pad to output pad	(fast)	15	T_{RPO}		33.0		29.0			ns
	(slew-rate limited)	15	T_{RPO}		43.0		37.0			ns

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). For larger capacitive loads, see page XAPP024. Typical slew rate limited output rise/fall times are approximately four times longer.

2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.

3. Input pad set-up time is specified with respect to the internal clock (IK). In order to calculate system set-up time, subtract clock delay (pad to IK) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (IK) is *negative*. This means that pad level changes immediately before the internal clock edge (IK) will not be recognized.

4. T_{PID}, T_{PTG}, and T_{PICK} are 3 ns higher for XTL2 when the pin is configured as a user input.

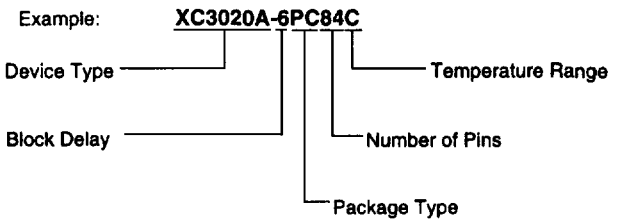
For a detailed description of the device architecture, see pages 2-105 through 2-123.

For a detailed description of the configuration modes and their timing, see pages 2-124 through 2-132.

For detailed lists of package pin-outs, see pages 2-140 through 2-150.

For package physical dimensions and thermal data, see Section 4.

Ordering Information



Component Availability

PINS		44	64	68	84		100				132		144	160	164	175		176	208	223
TYPE		PLAST. PLCC	PLAST. VQFP	PLAST. PLCC	PLAST. PLCC	CERAM PGA	PLAST. PQFP	PLAST. TQFP	PLAST. VQFP	TOP-BRAZED CQFP	PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	TOP-BRAZED CQFP	PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	CERAM. PGA
CODE		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	CB100	PP132	PG132	TQ144	PQ160	CB164	PP175	PG175	TQ176	PQ208	PG223
XC3020A	-7			C I	C I	C I	C I													
	-6			C	C	C	C													
XC3030A	-7	C I	C I	C I	C I	C I	C I		C I											
	-6	C	C	C	C	C	C		C											
XC3042A	-7				C I	C I	C I		C I		C I	C I	C I							
	-6				C	C	C		C		C	C	C							
XC3064A	-7				C I						C I	C I	C I	C I						
	-6				C						C	C	C	C						
XC3090A	-7				C I									C I		C I	C I	C I	C I	
	-6				C									C		C	C	C	C	

C = Commercial = 0° to +85° C I = Industrial = -40° to +100° C M = Mil Temp = -55° to +125° C B = MIL-STD-883C Class B

XC3000L Low Voltage Logic Cell Array Family

Product Specifications

Features

- Part of the ZERO+ family of 3.3 V FPGAs
- Low supply voltage FPGA family with five device types
  - JEDEC-compliant 3.3 V version of theXC3000A LCA Family
  - Logic densities from 1,000 to 6,000 gates
  - Up to 144 user-definable I/Os
- Advanced, low power 0.8 µ CMOS static memory technology
  - Very low quiescent current consumption, ≤ 20µA
  - Operating power consumption 56% less than XC3000A, 66% less than previous generation 5 V FPGAs
- Superset of the industry-leading XC3000 family
  - Identical to the basic XC3000 in structure, pinout, design methodology, and software tools
  - 100% compatible with all XC3000, XC3000A, XC3100 and XC3100A bitstreams
  - Improved routing and additional features
- Additional programmable interconnection points (PIPs)
  - Improved access to Longlines and CLB clock enable inputs
  - Most efficient XC3000-class solution to bus-oriented designs
- XC3000L-specific features
  - Guaranteed over the 3.0 to 3.6 V Vcc range
  - 4 mA output sink and source current
  - Error checking of the configuration bitstream
  - Soft startup starts all outputs in slew-limited mode upon power-up
  - Easy migration to the XC3400 series of HardWire mask programmed devices for high-volume production

Description

The XC3000L family of FPGAs is optimized for operation from a nominally 3.3 V supply. Aside from the electrical and timing parameters listed in this data sheet, the XC3000L family is in all respects identical with the XC3000A family, and is a superset of the XC3000 family.

The operating power consumption of Xilinx FPGAs is almost exclusively dynamic, and it changes with the square of the supply voltage. For a given complexity and clock speed, the XC3000L consumes, therefore, only 44% of the power used by the equivalent XC3000A device. In accordance with its use in battery-powered equipment, the XC3000L family was designed for the lowest possible power-down and quiescent current consumption.

In mixed supply-voltage systems, the XC3000L, fed by a 3.3 V (nominal) supply, can directly drive any device with TTL-like input thresholds. When a 5 V device drives the XC3000L, a current-limiting resistor (1 kΩ) or a voltage divider is required to prevent excessive input current.

Like the XC3000A family, XC3000L offers the following functional improvements over the popular XC3000 family:

The XC3000L family has additional interconnect resources to drive the I-inputs of TBUFs driving horizontal Longlines. The CLB Clock Enable input can be driven from a second vertical Longline. These two additions result in more efficient and faster designs when horizontal Longlines are used for data bussing.

During configuration, the XC3000L devices check the bitstream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls INIT Low.

When the configuration process is finished and the device starts up in user mode, the first activation of the outputs is automatically slew-rate limited. This feature, called Soft Startup, avoids the potential ground bounce when all outputs are turned on simultaneously. After start-up, the slew rate of the individual outputs is, as in the XC3000 family, determined by the individual configuration option.

The XC3000L family is a superset of the XC3000 family. Any bitstream used to configure an XC3000 device configures an XC3000L device the same way.

Device	CLBs	Array	User I/Os Max	Flip-Flops	Horizontal Longlines	Configurable Data Bits
XC3020L	64	8 x 8	64	256	16	14,779
XC3030L	100	10 x 10	80	360	20	22,176
XC3042L	144	12 x 12	96	480	24	30,784
XC3064L	224	16 x 14	120	688	32	46,064
XC3090L	320	16 x 20	144	928	40	64,160

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
V_{IH}	High-level input voltage	2.0	V_{CC} +0.3	V
V_{IL}	Low-level input voltage	-0.3	0.8	V
T_{IN}	Input signal transition time		250	ns

At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.

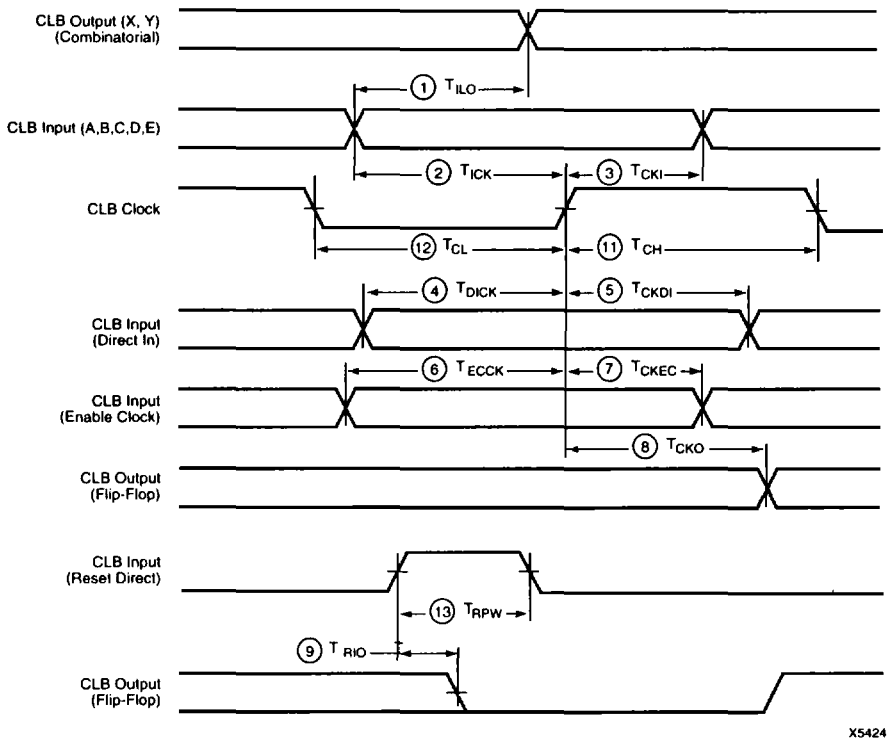
Although the present (1994) devices operate over the full supply voltage range from 3.0 to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 to 3.6 V range later, when smaller device geometries might preclude operation at 5 V.

DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	2.40		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)		0.40	V
V_{OH}	High-level output voltage (@ –100 µA, V_{CC} min)	V_{CC} -0.2		V
V_{OL}	Low-level output voltage (@ 100 µA, V_{CC} min)		0.2	V
V_{CCPD}	Power-down supply voltage ($\overline{PWRDWN}$ must be Low)	2.30		V
I_{CCPD}	Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX})		10	µA
I_{CCO}	Quiescent LCA supply current* Chip thresholds programmed as CMOS levels		20	µA
I_{IL}	Input Leakage Current, all I/O pins in parallel	–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		 10 15	 pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		 15 20	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V (sample tested)	0.02	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		2.50	mA

* With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the LCA device configured with a MakeBits tie option. I_{CCO} is in addition to I_{CCPD}.

CLB Switching Characteristic Guidelines



Buffer (Internal) Switching Characteristic Guidelines

	Speed Grade	-8			
Description	**Symbol**	**Max**			**Units**
Global and Alternate Clock Distribution*					
Either: Normal IOB input pad through clock buffer to any CLB or IOB clock input	T_{PGC}	9.0			ns
Or: Fast (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PGCC}	7 .0			ns
TBUF driving a Horizontal Longline (L.L.)*					
I to L.L. while T is Low (buffer active)	T_{IO}	5 .0			ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	12 .0			ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	24 .0			ns
BIDI					
Bidirectional buffer delay	T_{BIDI}	2 .0			ns

* Timing is based on the XC3042L, for other devices see XACT timing calculator.
Note: The use of two pull-up resistors per Longline, available on other XC3000 devices, is not a valid design option for XC3000L devices

CLB Switching Characteristic Guidelines (continued)

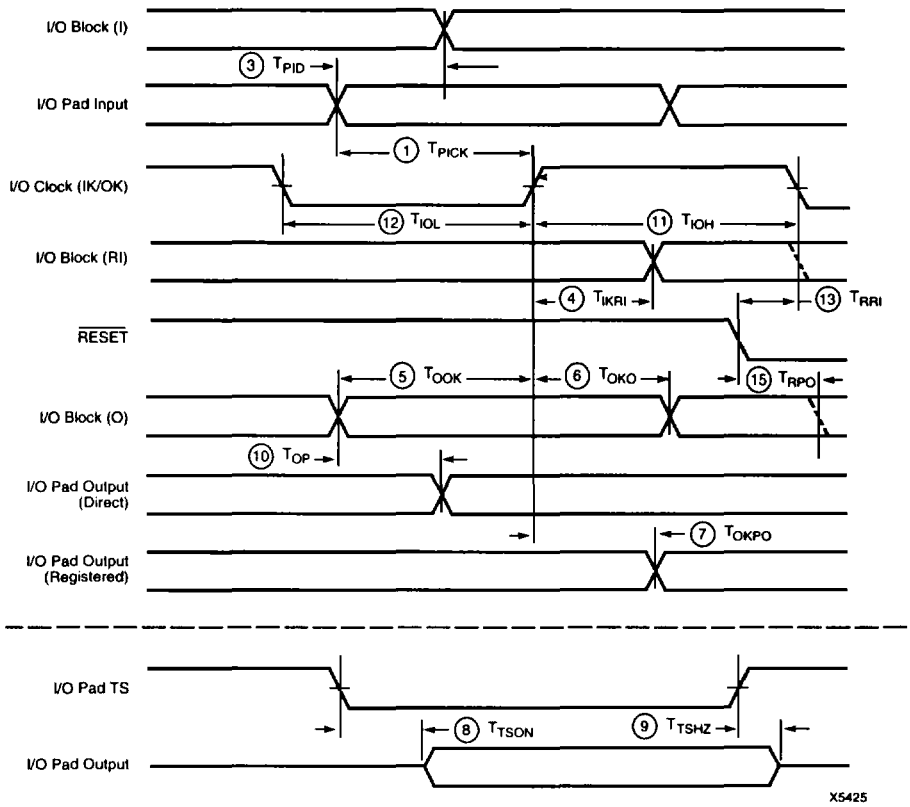
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

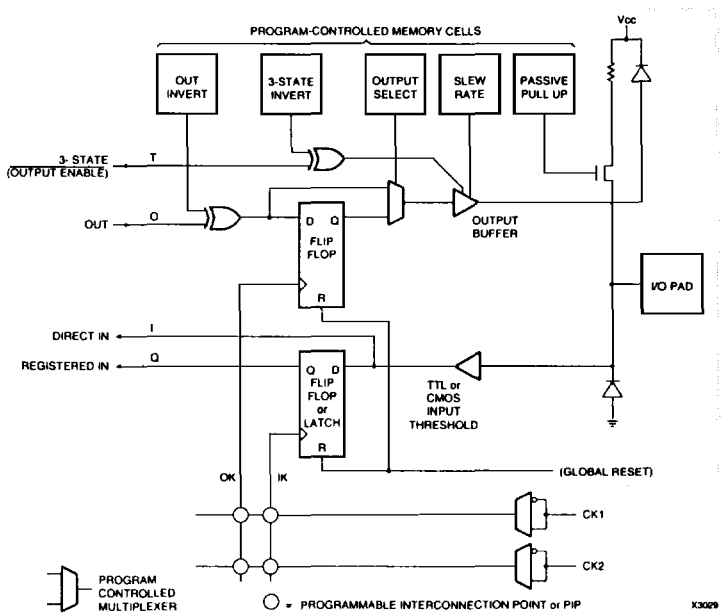
Speed Grade			-8							
Description	**Symbol**		**Min**	**Max**						**Units**
Combinatorial Delay										
Logic Variables A, B, C, D, E, to outputs X or Y										
FG Mode	1	T_{ILO}		6.7						ns
F and FGM Mode				7.5						ns
Sequential delay										
Clock k to outputs X or Y	8	T_{CKO}		7.5						ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y										
FG Mode		T_{QLO}		14.0						ns
F and FGM Mode				14.8						ns
Set-up time before clock K										
Logic Variables A, B, C, D, E										
FG MODE	2	T_{ICK}	5.0							ns
F and FGM Mode			5.8							ns
Data In DI	4	T_{DICK}	5.0							ns
Enable Clock EC	6	T_{ECCK}	5.0							ns
Hold Time after clock K										
Logic Variables A, B, C, D, E	3	T_{CKI}	0							ns
Data In DI	5	T_{CKDI}	2.0							ns
Enable Clock EC	7	T_{CKEC}	2.0							ns
Clock										
Clock High time	11	T_{CH}	5.0							ns
Clock Low time	12	T_{CL}	5.0							ns
Max. flip-flop toggle rate		F_{CLK}	80.0							MHz
Reset Direct (RD)										
RD width	13	T_{RPW}	7.0							ns
delay from RD to outputs X or Y	9	T_{RIO}	7.0							ns
Global Reset ($\overline{\text{RESET}}$ Pad)*										
$\overline{\text{RESET}}$ width (Low)		T_{MRW}	16.0							ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y		T_{MRQ}		23.0						ns

*Timing is based on the XC3042A, for other devices see XACT timing calculator.

Notes: The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

IOB Switching Characteristic Guidelines





IOB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade		-8						
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Propagation Delays (Input)									
Pad to Direct In (I)	3	T_{PID}		5.0					ns
Pad to Registered In (Q) with latch transparent		T_{PTG}		24.0					ns
Clock (IK) to Registered In (Q)	4	T_{IKRI}		6.0					ns
Set-up Time (Input)									
Pad to Clock (IK) set-up time	1	T_{PICK}	22.0						ns
Propagation Delays (Output)									
Clock (OK) to Pad (fast)	7	T_{OKPO}		12.0					ns
same (slew rate limited)	7	T_{OKPO}		28.0					ns
Output (O) to Pad (fast)	10	T_{OPF}		9.0					ns
same (slew-rate limited)	10	T_{OPS}		25.0					ns
3-state to Pad begin hi-Z (fast)	9	T_{TSHZ}		12.0					ns
same (slew-rate limited)	9	T_{TSHZ}		28.0					ns
3-state to Pad active and valid (fast)	8	T_{TSON}		16.0					ns
same (slew -rate limited)	8	T_{TSON}		32.0					ns
Set-up and Hold Times (Output)									
Output (O) to clock (OK) set-up time	5	T_{OOK}	12.0						ns
Output (O) to clock (OK) hold time	6	T_{OKO}	0						ns
Clock									
Clock High time	11	T_{IOH}	5.0						ns
Clock Low time	12	T_{IOL}	5.0						ns
Max. flip-flop toggle rate		F_{CLK}	80.0						MHz
Global Reset Delays (based on XC3042L)									
$\overline{\text{RESET}}$ Pad to Registered In (Q)	13	T_{RRI}	25.0						ns
$\overline{\text{RESET}}$ Pad to output pad (fast)	15	T_{RPO}	35.0						ns
(slew-rate limited)	15	T_{RPO}	51.0						ns

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). For larger capacitive loads, see page XAPP024. Typical slew rate limited output rise/fall times are approximately four times longer.

2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.

3. Input pad set-up time is specified with respect to the internal clock (IK). In order to calculate system set-up time, subtract clock delay (pad to IK) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (IK) is negative. This means that pad level changes immediately before the internal clock edge (IK) will not be recognized.

4. The slew-limited delays for T_{OKPO}, T_{SHZ}, T_{TSON}, and T_{RPO} are guaranteed by design and not tested.

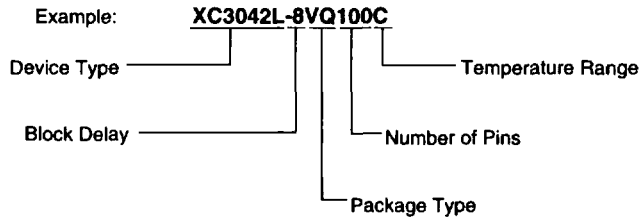
For a detailed description of the device architecture, see pages 2-105 through 2-123.

For a detailed description of the configuration modes and their timing, see pages 2-124 through 2-132.

For detailed lists of package pin-outs, see pages 2-140 through 2-150.

For package physical dimensions and thermal data, see Section 4.

Ordering Information



Component Availability

PINS	44	64	68	84		100				132		144	160	164	175		176	208	223
TYPE	PLAST. PLCC	PLAST. VQFP	PLAST. PLCC	PLAST. PLCC	CERAM PGA	PLAST. PQFP	PLAST. TQFP	PLAST VQFP	TOP-BRAZED CQFP	PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	TOP-BRAZED CQFP	PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	CERAM. PGA
CODE	PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	CB100	PP132	PG132	TQ144	PQ160	CB164	PP175	PG175	TQ176	PQ208	PG223
XC3020L				C															
XC3030L		C		C				C											
XC3042L				C				C				C							
XC3064L				C								C							
XC3090L				C													C		

C = Commercial = 0° to +70° C I = Industrial = -40° to +85° C M = Mil Temp = -55° to +125° C B = MIL-STD-883C Class B

XC3100A
Logic Cell Array Families

Product Specifications

Features

- Ultra-high-speed FPGA family with six members
  - 50-85 MHz system clock rates
  - 190 to 325 MHz guaranteed flip-flop toggle rates
  - 1.75 to 4.1 ns logic delays
- High-end additional family member in the 22 X 22 CLB array-size XC3195A device
- 8 mA output sink current and 8 mA source current
- Maximum power-down and quiescent current is 5 mA
- Both families are 100% architecture and pin-out compatible with other XC3000 families
- Beyond this, XC3100A is also software and bitstream compatible with the XC3000, XC3000A, and XC3000L families
- 100% PCI complaint (A-2 speed grade in plastic quad flat pack (PQFP) packaging).

XC3100A combines the features of the XC3000A and XC3100 families.

- Additional interconnect resources for TBUFs and CE inputs
- Error checking of the configuration bitstream
- Soft startup holds all outputs slew-rate limited during initial power-up
- More advanced CMOS process

Description

The XC3100A is a performance-optimized relative of the XC3000 and XC3000A families. While all families are footprint compatible, XC3100A familiy extends the system performance beyond 80 MHz.

The XC3100A familiy follows the XC4000 speed-grade nomenclature, indicating device performance with a number that is based on the internal logic-block delay, in ns.

The XC3100A family offers the following enhancements over the popular XC3100 family.

The XC3100A family has additional interconnect resources to drive the I-inputs of TBUFs driving horizontal Longlines. The CLB Clock Enable input can be driven from a second vertical Longline. These two additions result in more efficient and faster designs when horizontal Longlines are used for data bussing.

During configuration, the XC3100A devices check the bitstream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls INIT Low.

When the configuration process is finished and the device starts up in user mode, the first activation of the outputs is automatically slew-rate limited. This feature, called Soft Startup, avoids the potential ground bounce when all outputs are turned on simultaneously. After start-up, the slew rate of the individual outputs is, as in all XC3000 families, determined by the individual configuration option.

The XC3100A family is a superset of the XC3000 families. Any bitstream used to configure an XC3000, XC3000A, XC3000L or XC3100 device, will configure the same-size XC3100A device exactly the same way.

Device	CLBs	Array	User I/O Max	Flip-Flops	Horizontal Longlines	Configuration Data Bits
XC3120A	64	8 x 8	64	256	16	14,779
XC3130A	100	10 x 10	80	360	20	22,176
XC3142A	144	12 x 12	96	480	24	30,784
XC3164A	224	16 x 14	120	688	28	46,064
XC3190A	320	16 x 20	144	928	40	64,160
XC3195A	484	22 x 22	176	1,320	44	94,944

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial -40°C to +100°C junction	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration	2.0	V_{CC}	V
V_{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration	70%	100%	V_{CC}
V_{ILC}	Low-level input voltage — CMOS configuration	0	20%	V_{CC}
T_{IN}	Input signal transition time		250	ns

At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.

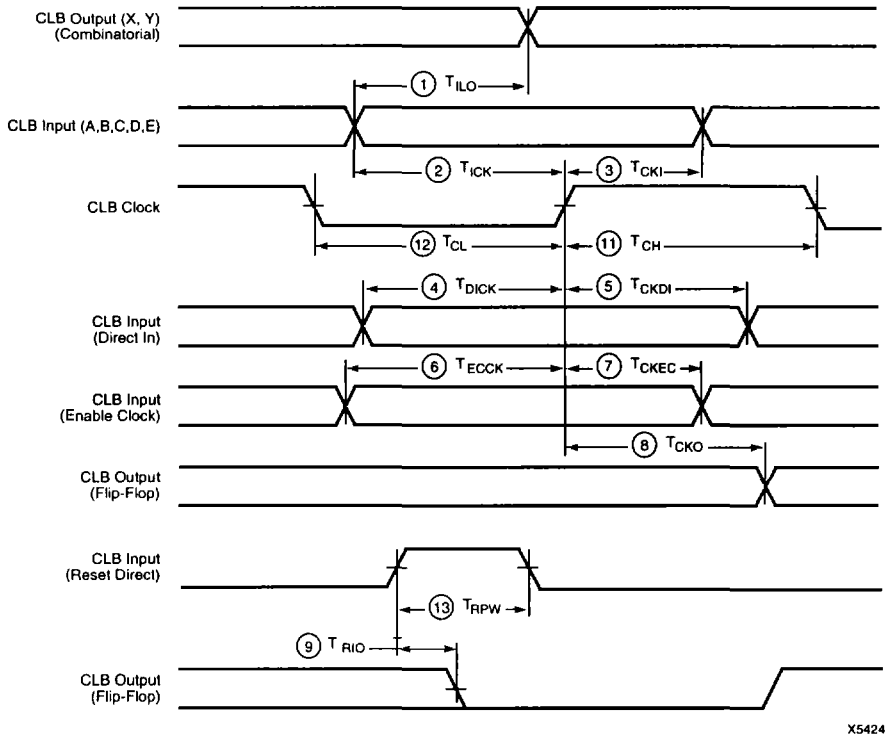
DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –8.0 mA, V_{CC} min)	Commercial	3.86		V
V_{OL}	Low-level output voltage (@ I_{OL} = 8.0 mA, V_{CC} min)			0.40	V
V_{OH}	High-level output voltage (@ I_{OH} = –8.0 mA, V_{CC} min)	Industrial	3.76		V
V_{OL}	Low-level output voltage (@ I_{OL} = 8.0 mA, V_{CC} min)			0.40	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)		2.30		V
I_{CCO}	Quiescent LCA supply current Chip thresholds programmed as CMOS levels[1]			8	mA
	Chip thresholds programmed as TTL levels			14	mA
I_{IL}	Input Leakage Current		–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 10 15	 pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 15 20	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	0.17	mA
I_{RLL}	Horizontal long line pull-up (when selected) @ logic Low		0.20	2.80	mA

Note: 1. With no output current loads, no active input or long line pull-up resistors, all package pins at V_{CC} or GND, and the LCA configured with a MakeBits tie option.

2. Total continuous output sink current may not exceed 100 mA per ground pin. The number of ground pins varies from two for the XC3120A in the PC84 package, to eight for the XC3195A in the PQ208 or PG223 package.

CLB Switching Characteristic Guidelines



Buffer (Internal) Switching Characteristic Guidelines

Speed Grade		-5	-4	-3	-2	-1	
Description	**Symbol**	**Max**	**Max**	**Max**	**Max**	**Max**	**Units**
Global and Alternate Clock Distribution*							
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	6.8	6.5	5.6	5.2	3.8	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	5.4	5.1	4.3	4.0	3.3	ns
TBUF driving a Horizontal Long line (L.L.)*							
I to L.L. while T is Low (buffer active) (XC3100)	T_{IO}	4.1	3.7	3.1			ns
(XC3100A)	T_{IO}	3.6	3.6	3.1	3.1	2.8	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	5.6	5.0	4.2	4.2	3.9	ns
T↓ to L.L. active and valid with pair of pull-up resistors	T_{ON}	7.1	6.5	5.7	5.7	5.4	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	15.6	13.5	11.4	11.4	10.3	ns
T↑ to L.L. High with pair of pull-up resistors	T_{PUF}	12.0	10.5	8.8	8.1	7.0	ns
BIDI							
Bidirectional buffer delay	T_{BIDI}	1.4	1.2	1.0	0.9	0.85	ns

* Timing is based on the XC3142A, for other devices see XACT timing calculator.

CLB Switching Characteristic Guidelines (continued)

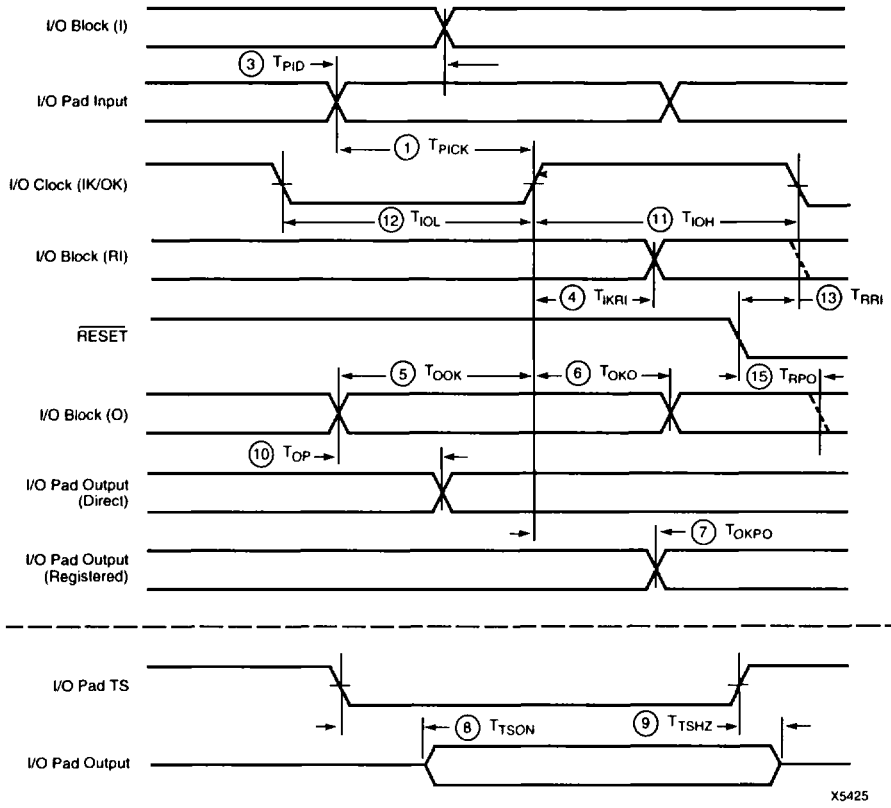
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

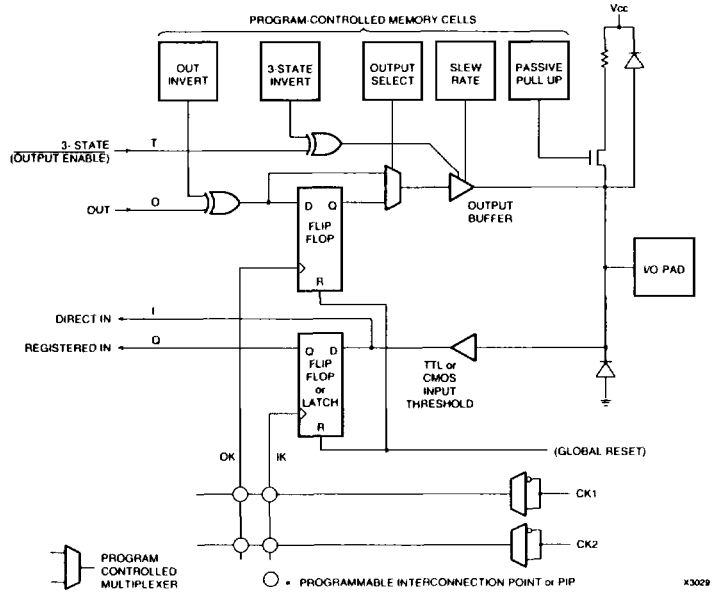
Speed Grade			-5		-4		-3		-2		-1		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delay													
Logic Variables A, B, C, D, E, to outputs X or Y	1	T_{ILO}		4.1		3.3		2.7		2.2		1.75	ns
Sequential delay													
Clock K to outputs X or Y	8	T_{CKO}		3.1		2.5		2.1		1.7		1.4	ns
Clock K to outputs X or Y when Q is returned through function generators F or G to drive X or Y		T_{QLO}		6.3		5.2		4.3		3.5	3.1		ns
Set-up time before clock K													
Logic Variables A, B, C, D, E	2	T_{ICK}	3.1		2.5		2.1		1.8		1.7		ns
Data In DI	4	T_{DICK}	2.0		1.6		1.4		1.3		1.2		ns
Enable Clock EC	6	T_{ECCK}	3.8		3.2		2.7		2.5		2.3		ns
Reset Direct inactive RD			1.0		1.0		1.0		1.0		1.0		ns
Hold Time after clock k													
Logic Variables A, B, C, D, E	3	T_{CKI}	0		0		0		0		0		ns
Data In DI	5	T_{CKDI}	1.0		1.0		0.9		0.9		0.8		ns
Enable Clock EC	7	T_{CKEC}	1.0		0.8		0.7		0.7		0.6		ns
Clock													
Clock High time	11	T_{CH}	2.4		2.0		1.6		1.3		1.3		ns
Clock Low time	12	T_{CL}	2.4		2.0		1.6		1.3		1.3		ns
Max. flip-flop toggle rate		F_{CLK}	190		230		270		325		325		MHz
Reset Direct (RD)													
RD width	13	T_{RPW}	3.8		3.2		2.7		2.3		2.3		ns
delay from RD to outputs X or Y	9	T_{RIO}		4.4		3.7		3.1		2.7		2.4	ns
Global Reset, from $\overline{\text{RESET}}$ Pad,													
$\overline{\text{RESET}}$ width (Low) (XC3142A)		T_{MRW}	14.0		14.0		12.0		12.0		12.0		ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y		T_{MRQ}		17.0		14.0		12.0		12.0		12.0	ns

Notes: The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

T_{ILO}, T_{QLO} and T_{ICK} are specified for 4-input functions. For 5-input functions or base FGM functions, each of these specifications for the XC3100A family increses by 0.50 ns (-5), 0.42 ns (-4) and 0.35 ns (-3).

IOB Switching Characteristic Guidelines





IOB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

Speed Grade			-5		-4		-3		-2		-1		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Propagation Delays (Input)													
Pad to Direct In (I)	3	T_{PID}		2.8		2.5		2.2		2.0		1.7	ns
Pad to Registered In (q) with													
latch transparent (XC3100A)		T_{PTG}		14.0		12.0		11.0		11.0		10.0	ns
(XC3100)		T_{PTG}		16.0		15.0		13.0					ns
Clock (IK) to Registered In (Q)	4	T_{IKRI}		2.8		2.5		2.2		1.9		1.7	ns
Set-up Time (Input)													
Pad to Clock (IK) set-up time													
XC3100 Family	1	T_{PICK}	15.0		14.0		12.0						ns
XC3120A,XC3130A			10.9		10.6		9.4		8.9		8.0		ns
XC3142A			11.0		10.7		9.5		9.0		8.1		ns
XC3164A			11.2		11.0		9.7		9.2		8.3		ns
XC3190A			11.5		11.2		9.9		9.4		8.5		ns
XC3195A			12.0		11.6		10.3		9.8		8.9		ns
Propagation Delays (Output)													
Clock (OK) to Pad (fast)	7	T_{OKPO}		5.5		5.0		4.4		4.0		3.4	ns
same (slew-rate limited)	7	T_{OKPO}		14.0		12.0		10.0		9.7		8.4	ns
Output (O) to Pad (fast)	10	T_{OPF}		4.1		3.7		3.3		3.0		3.0	ns
same (slew-rate limited) (XC3100A)	10	T_{OPS}		12.1		11.0		9.0		8.7		8.0	ns
(XC3100)	10	T_{OPF}		13.0		11.0		9.0					ns
3-state to Pad begin hi-Z (fast)	9	T_{TSHZ}		6.9		6.2		5.5		5.0		4.5	ns
same (slew-rate limited)	9	T_{TSHZ}		6.9		6.2		5.5		5.0		4.5	ns
3-state to Pad active and valid (fast) (XC3100A)	8	T_{TSON}		10.0		10.0		9.0		8.5		6.5	ns
same (slew-rate limited)	8	T_{TSON}		18.0		17.0		15.0		14.2		11.5	ns
3-state to Pad active and valid (fast) (XC3100)	8	T_{TSON}		12.0		10.0		9.0					ns
same (slew-rate limited)	8	T_{TSON}		20.0		17.0		15.0					ns
Set-up and Hold Times (Output)													
Output (O) to clock (OK) set-up time,(XC3100A)	5	T_{OOK}	5.0		4.5		4.0		3.6		3.2		ns
(XC3100)	5	T_{OOK}	6.2		5.6		5.0						ns
Output (O) to clock (OK) hold time	6	T_{OKO}	0		0		0		0		0		ns
Clock													
Clock High time	11	T_{IOH}	2.4		2.0		1.6		1.3		1.3		ns
Clock Low time	12	T_{IOL}	2.4		2.0		1.6		1.3		1.3		ns
Max. flip-flop toggle rate		F_{CLK}	190.0		230.0		270.0		325.0		325.0		MHz
Global Reset Delays													
RESET Pad to Registered In (Q),													
(XC3120/XC3120A)	13	T_{RRI}		18.0		15.0		13.0		13.0		13.0	ns
(XC3195/XC3195A)				29.5		25.0		21.0		21.0		21.0	ns
RESET Pad to output pad (fast)	15	T_{RPO}		24.0		20.0		17.0		17.0		17.0	ns
(slew-rate limited)	15	T_{RPO}		32.0		27.0		23.0		23.0		22.0	ns

Notes:
1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). For larger capacitive loads, see XAPP 024. Typical slew rate limited output rise/fall times are approximately four times longer.
2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
3. Input pad set-up time is specified with respect to the internal clock (IK). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (IK) is negative. This means that pad level changes immediately before the internal clock edge (IK) will not be recognized.
4. T_{PID}, T_{PTG}, and T_{PICK} are 3 ns higher for XTAL2 when the pin is configured as a user input.

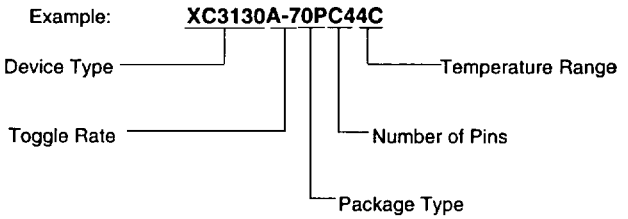
For a detailed description of the device architecture, see pages 2-105 through 2-123.

For a detailed description of the configuration modes and their timing, see pages 2-124 through 2-132.

For detailed lists of package pin-outs, see pages 2-140 through 2-150.

For package physical dimensions and thermal data, see Section 4.

Ordering Information



Component Availability

PINS		44	64	68	84		100				132		144	160	164	175		176	208	223
TYPE		PLAST. PLCC	PLAST. VQFP	PLAST. PLCC	PLAST. PLCC	CERAM PGA	PLAST. PQFP	PLAST TQFP	PLAST. VQFP	TOP-BRAZED CQFP	PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	TOP-BRAZED CQFP	PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	CERAM. PGA
CODE		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	CB100	PP132	PG132	TQ144	PQ160	CB164	PP175	PG175	TQ176	PQ208	PG223
XC3120A	-5			C I	C I	C I	C I													
	-4			C I	C I	C I	C I													
	-3			C I	C I	C I	C I													
	-2			C	C	C	C													
	-1			C	C	C	C													
XC3130A	-5	C I		C I	C I	C I	C I		C											
	-4	C I		C I	C I	C I	C I		C											
	-3	C I		C I	C I	C I	C I		C											
	-2	C		C	C	C	C		C											
	-1	C		C	C	C	C		C											
XC3142A	-5				C I	C I M B	C I		C	M B	C	C I M B	C I							
	-4				C I	C I	C I		C		C	C I	C I							
	-3				C I	C I	C I		C		C	C I	C I							
	-2				C	C	C		C		C	C	C							
	-1				C	C	C		C		C	C	C							
XC3164A	-5				C I						C I	C I	C I	C I						
	-4				C I						C I	C I	C I	C I						
	-3				C I						C I	C I	C I	C I						
	-2				C						C	C	C	C						
	-1				C						C	C	C	C						
XC3190A	-5				C I									C I	M B	C I	C I M B	C I	C I	
	-4				C I									C I		C I	C I	C I	C I	
	-3				C I									C I		C I	C I	C I	C I	
	-2				C									C		C	C	C	C	
	-1				C									C		C	C	C	C	
XC3195A	-5				C I									C I	M B	C I	C I M B		C I	C I M B
	-4				C I									C I		C I	C I		C I	C I
	-3				C I									C I		C I	C I		C I	C I
	-2				C									C		C	C		C	C
	-1				C									C		C	C		C	C

C = Commercial = 0° to +85° C I = Industrial = -40° to +100° C M = Mil Temp = -55° to +125° C B = MIL-STD-883C Class B

Parentheses indicate future product plans